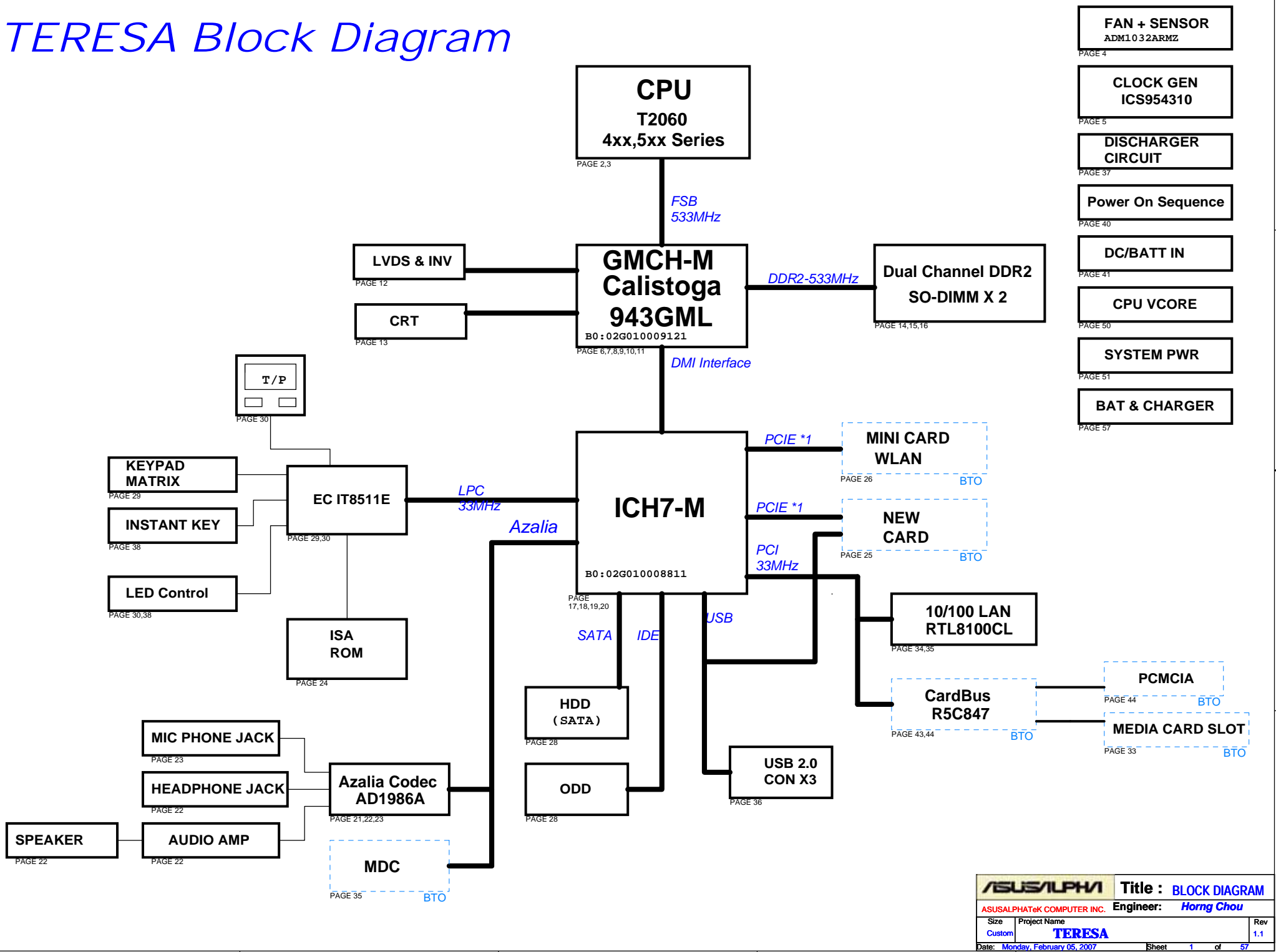
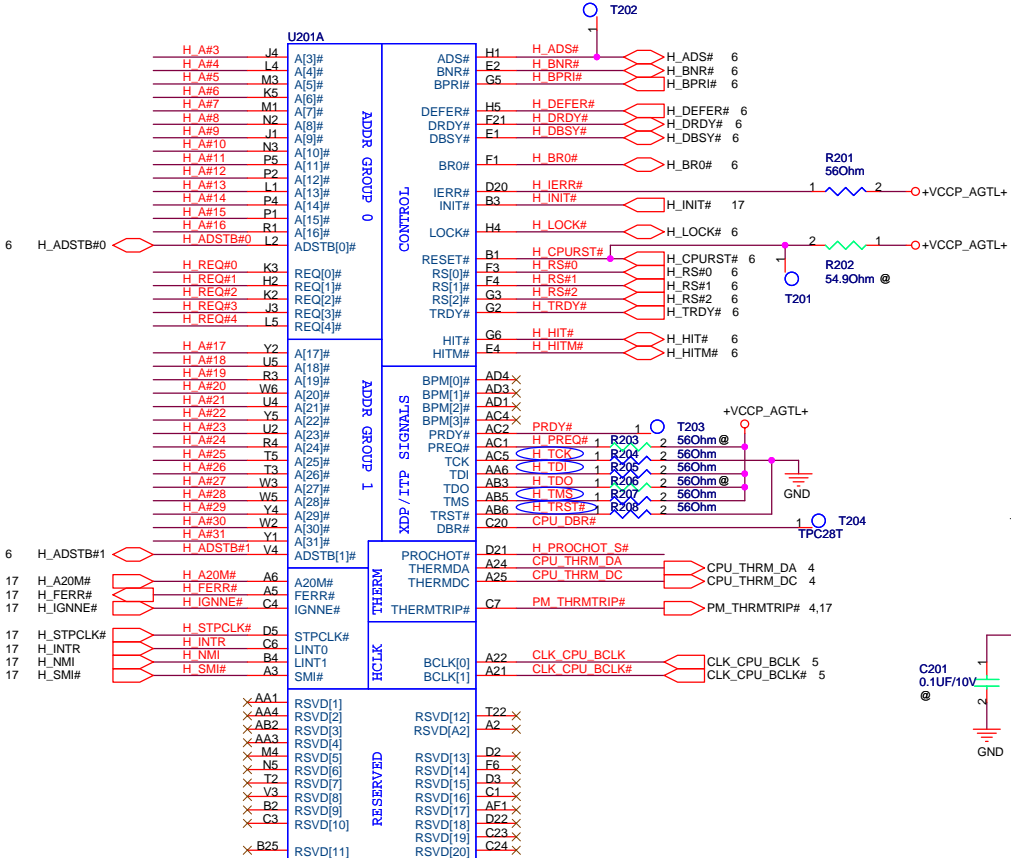


TERESA Block Diagram

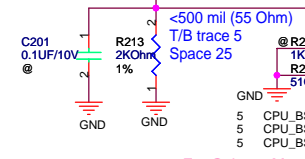
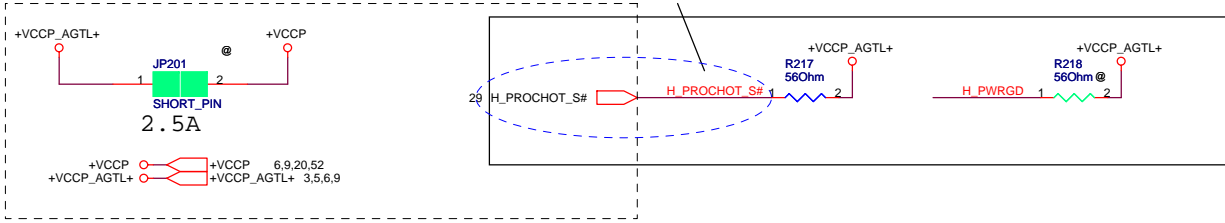


6 H_A#[16..3]
 6 H_REQ#[4..0]
 6 H_A#[31..17]



(070122)Change CPU Socket into PN=12G011204796

68 ± 5% pull-up to Vcc1_05
 If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
 If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ± 5%



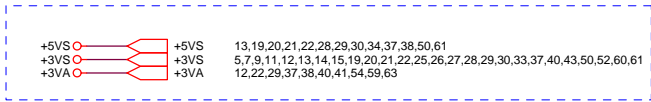
For Celeron M

BCLK	FSB	BSEL2	BSEL1	BSEL0
133MHZ	533MHZ	L	L	H

(070122)Change CPU Socket into PN=12G011204796

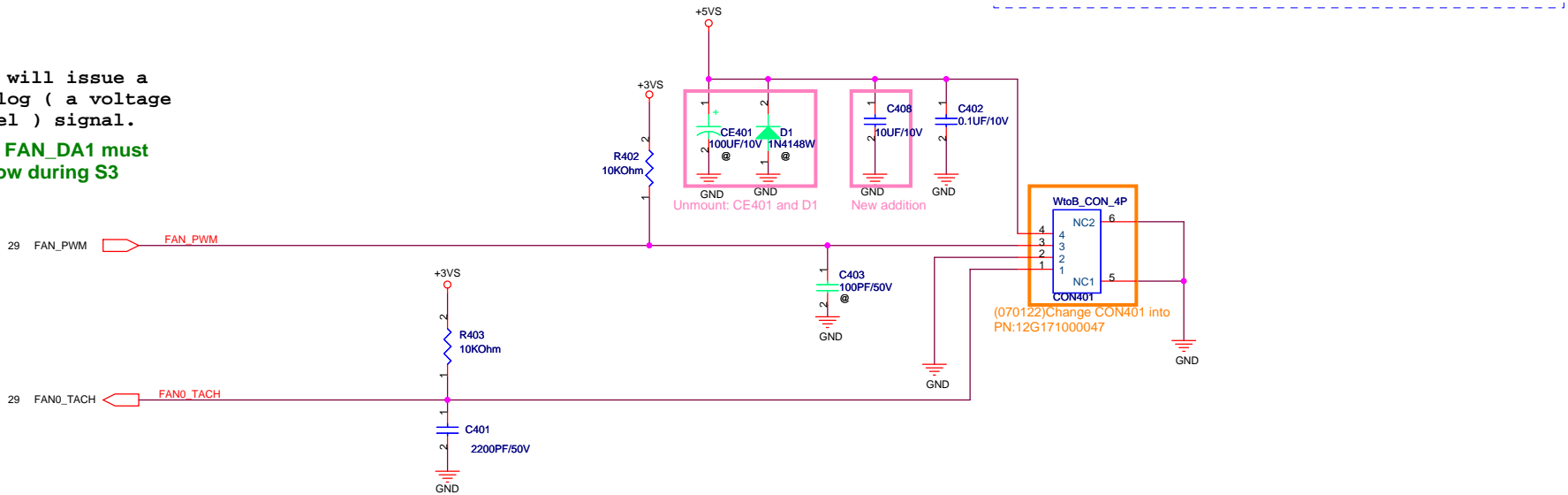
Layout Note:
 Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
 Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
 Comp(3:0) at least 25 mils away from any other toggling signal.
 27.4 ohm connects with an ~18mil wide trace to comp0.
 54.9 ohm connect with 5mil-wide trace to comp1

Fan Speed Control



KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3



THERMAL PROTECTION PLACE UNDER CPU (85 DEGREE C)

105 -> 85, R411 need to be tuned (1204) maybe R411=14.7K Ohm(10G213147213010)

061214) Add 4 thermistors

7 GMCH_THRMTRIP# 1 R417 0Ohm (070130) Add 0ohm resistor

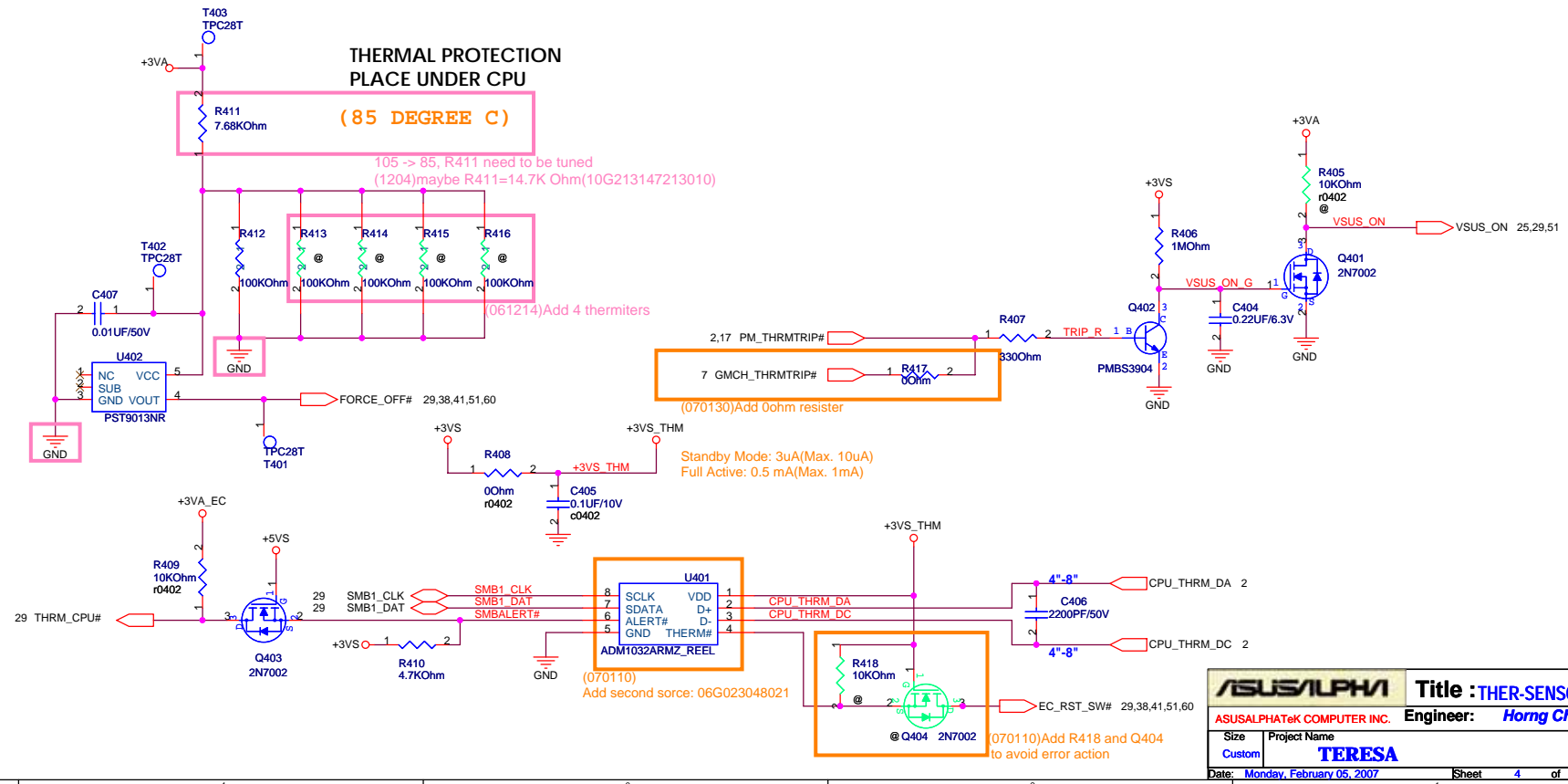
Standby Mode: 3uA(Max. 10uA)
Full Active: 0.5 mA(Max. 1mA)

(070110) Add R418 and Q404 to avoid error action

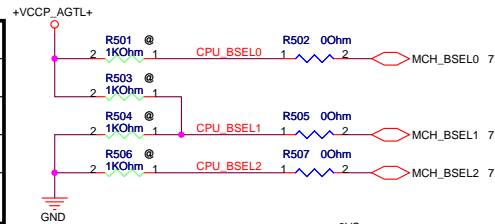
Route H_THERMDA and H_THERMDC on the same layer

-----OTHER SIGNALS
12 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
12 mils
-----OTHER SIGNALS

Avoid BPSB,Power



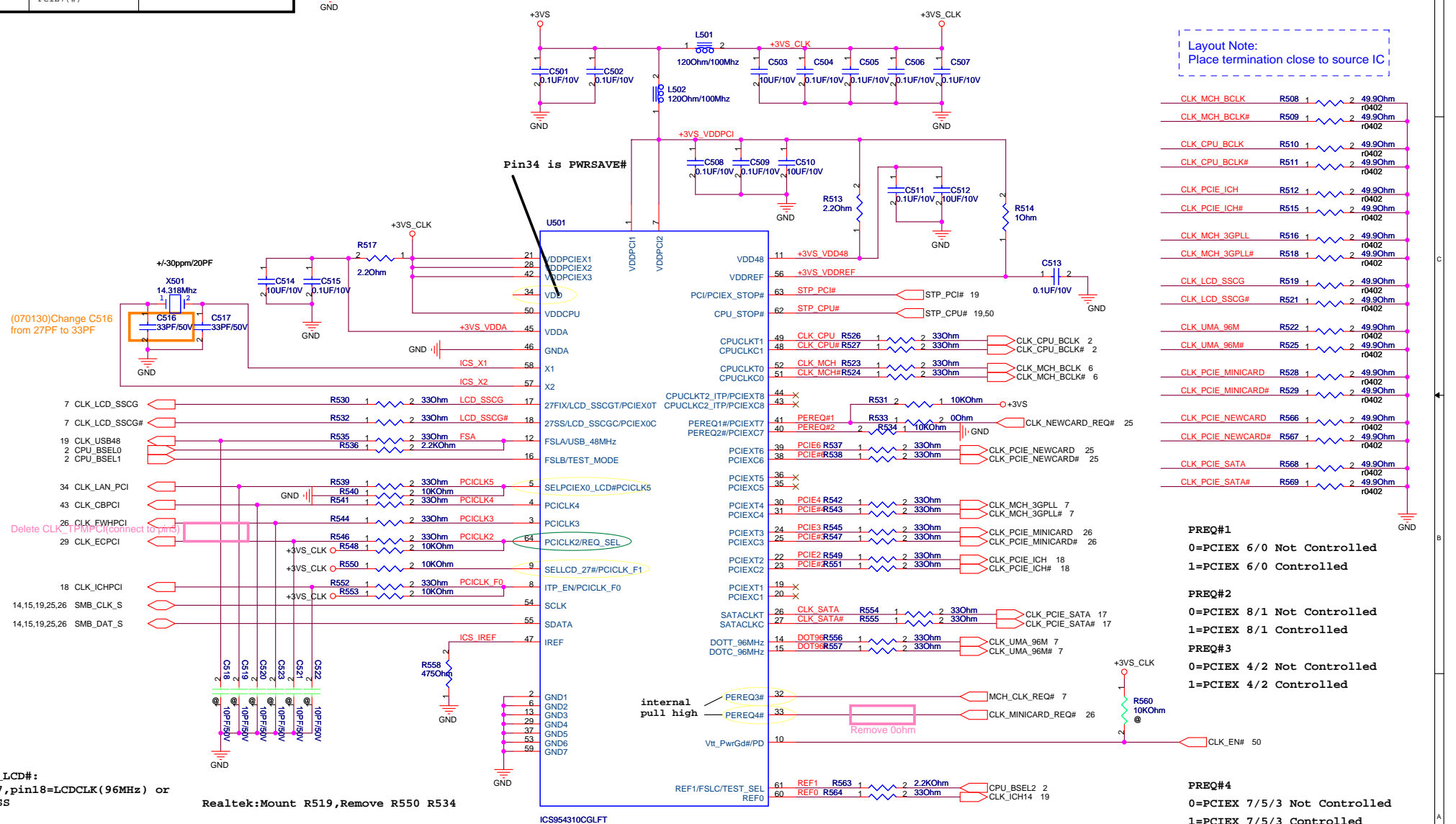
Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#),PCIE7(#)	CLK_MCH_3GPLL(#)



Bclk	F5B	F5LC	F5LB	F5LA
133	533	L	L	H
166	667	L	H	H



Layout Note:
Place termination close to source IC



CLK MCH_BCLK	R508	1	2	49.9Ohm	r0402
CLK MCH_BCLK#	R509	1	2	49.9Ohm	r0402
CLK CPU_BCLK	R510	1	2	49.9Ohm	r0402
CLK CPU_BCLK#	R511	1	2	49.9Ohm	r0402
CLK PCIE_ICH	R512	1	2	49.9Ohm	r0402
CLK PCIE_ICH#	R515	1	2	49.9Ohm	r0402
CLK MCH_3GPLL	R516	1	2	49.9Ohm	r0402
CLK MCH_3GPLL#	R518	1	2	49.9Ohm	r0402
CLK LCD_SSCG	R519	1	2	49.9Ohm	r0402
CLK LCD_SSCG#	R521	1	2	49.9Ohm	r0402
CLK UMA_96M	R522	1	2	49.9Ohm	r0402
CLK UMA_96M#	R525	1	2	49.9Ohm	r0402
CLK PCIE_MINICARD	R528	1	2	49.9Ohm	r0402
CLK PCIE_MINICARD#	R529	1	2	49.9Ohm	r0402
CLK PCIE_NEWCARD	R566	1	2	49.9Ohm	r0402
CLK PCIE_NEWCARD#	R567	1	2	49.9Ohm	r0402
CLK PCIE_SATA	R568	1	2	49.9Ohm	r0402
CLK PCIE_SATA#	R569	1	2	49.9Ohm	r0402

PREQ#1
0=PCIE 6/0 Not Controlled
1=PCIE 6/0 Controlled

PREQ#2
0=PCIE 8/1 Not Controlled
1=PCIE 8/1 Controlled

PREQ#3
0=PCIE 4/2 Not Controlled
1=PCIE 4/2 Controlled

PREQ#4
0=PCIE 7/5/3 Not Controlled
1=PCIE 7/5/3 Controlled

SELPCIE0_LCD#:
0-->pin17, pin18=LCDCLK(96MHz) or 27M/27M_SS

SELLCD_27#/PCICLK_F1:
1-->pin17, pin18=LCDCLK(96MHz)

PCICLK2/REQ_SEL:
1-->pin40, pin41=PREQ1#, PREQ2#

ITP_EN/PCICLK_F0:
1-->CPU_ITP pair

Realtek:Mount R519, Remove R550 R534

Internal Pull-Up Resistor

Internal Pull-Down Resistor

ASUS/ALPHA		Title : CLOCK GEN	
ASUSALPHATEK COMPUTER INC.		Engineer: Hong Chou	
Size Custom	Project Name TERESA	Date: Monday, February 05, 2007	Sheet 5 of 57
Rev 1.1			

2 H_D#[0..63]

H_A#[31..3] 2

U601A

H_D#0	F1	H_D#_0
H_D#1	J1	H_D#_1
H_D#2	H1	H_D#_2
H_D#3	J6	H_D#_3
H_D#4	H3	H_D#_4
H_D#5	K2	H_D#_5
H_D#6	G1	H_D#_6
H_D#7	G2	H_D#_7
H_D#8	K9	H_D#_8
H_D#9	K1	H_D#_9
H_D#10	K7	H_D#_10
H_D#11	J8	H_D#_11
H_D#12	H4	H_D#_12
H_D#13	J3	H_D#_13
H_D#14	K11	H_D#_14
H_D#15	G4	H_D#_15
H_D#16	T10	H_D#_16
H_D#17	W11	H_D#_17
H_D#18	T3	H_D#_18
H_D#19	U7	H_D#_19
H_D#20	U9	H_D#_20
H_D#21	U11	H_D#_21
H_D#22	T11	H_D#_22
H_D#23	W9	H_D#_23
H_D#24	T1	H_D#_24
H_D#25	T8	H_D#_25
H_D#26	T4	H_D#_26
H_D#27	W7	H_D#_27
H_D#28	U5	H_D#_28
H_D#29	T9	H_D#_29
H_D#30	W6	H_D#_30
H_D#31	T5	H_D#_31
H_D#32	AB7	H_D#_32
H_D#33	AA9	H_D#_33
H_D#34	W4	H_D#_34
H_D#35	W3	H_D#_35
H_D#36	Y3	H_D#_36
H_D#37	Y7	H_D#_37
H_D#38	W5	H_D#_38
H_D#39	Y10	H_D#_39
H_D#40	AB8	H_D#_40
H_D#41	W2	H_D#_41
H_D#42	AA4	H_D#_42
H_D#43	AA7	H_D#_43
H_D#44	AA2	H_D#_44
H_D#45	AA6	H_D#_45
H_D#46	AA10	H_D#_46
H_D#47	Y8	H_D#_47
H_D#48	AA1	H_D#_48
H_D#49	AB4	H_D#_49
H_D#50	AC9	H_D#_50
H_D#51	AB11	H_D#_51
H_D#52	AC11	H_D#_52
H_D#53	AB3	H_D#_53
H_D#54	AC2	H_D#_54
H_D#55	AD1	H_D#_55
H_D#56	AD9	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AD7	H_D#_58
H_D#59	AC6	H_D#_59
H_D#60	AB5	H_D#_60
H_D#61	AD10	H_D#_61
H_D#62	AD4	H_D#_62
H_D#63	AC8	H_D#_63

HOST

H_A#_3	H9	H_A#3
H_A#_4	C9	H_A#4
H_A#_5	E11	H_A#5
H_A#_6	G11	H_A#6
H_A#_7	F11	H_A#7
H_A#_8	G12	H_A#8
H_A#_9	F9	H_A#9
H_A#_10	H11	H_A#10
H_A#_11	J12	H_A#11
H_A#_12	G14	H_A#12
H_A#_13	D9	H_A#13
H_A#_14	J14	H_A#14
H_A#_15	H13	H_A#15
H_A#_16	I15	H_A#16
H_A#_17	F14	H_A#17
H_A#_18	D12	H_A#18
H_A#_19	A11	H_A#19
H_A#_20	C11	H_A#20
H_A#_21	A12	H_A#21
H_A#_22	A13	H_A#22
H_A#_23	E13	H_A#23
H_A#_24	G13	H_A#24
H_A#_25	F12	H_A#25
H_A#_26	B12	H_A#26
H_A#_27	C12	H_A#27
H_A#_28	A14	H_A#28
H_A#_29	C14	H_A#29
H_A#_30	D14	H_A#30
H_A#_31	C14	H_A#31

H_ADS#	E8	H_ADS#	2
H_ADSTB#0	B9	H_ADSTB#0	2
H_ADSTB#1	C13	H_ADSTB#1	2
H_VREF	J13	H_VREF	
H_BNR#	C6	H_BNR#	2
H_BPRI#	F6	H_BPRI#	2
H_BR0#	C7	H_BR0#	2
H_CPURST#	B7	H_CPURST#	2
H_DBSY#	A7	H_DBSY#	2
H_DEFER#	C3	H_DEFER#	2
H_DPWR#	J9	H_DPWR#	2
H_DRDY#	H8	H_DRDY#	2
H_DVREF	K13		

H_DINV#0	J7	H_DINV#0	2
H_DINV#1	W8	H_DINV#1	2
H_DINV#2	U3	H_DINV#2	2
H_DINV#3	AB10	H_DINV#3	2

H_DSTBN#0	K4	H_DSTBN#0	2
H_DSTBN#1	I7	H_DSTBN#1	2
H_DSTBN#2	Y5	H_DSTBN#2	2
H_DSTBN#3	AC4	H_DSTBN#3	2

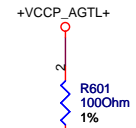
H_DSTBP#0	K3	H_DSTBP#0	2
H_DSTBP#1	T6	H_DSTBP#1	2
H_DSTBP#2	AA5	H_DSTBP#2	2
H_DSTBP#3	AC5	H_DSTBP#3	2

H_HIT#	D3	H_HIT#	2
H_HITM#	D4	H_HITM#	2
H_LOCK#	B3	H_LOCK#	2

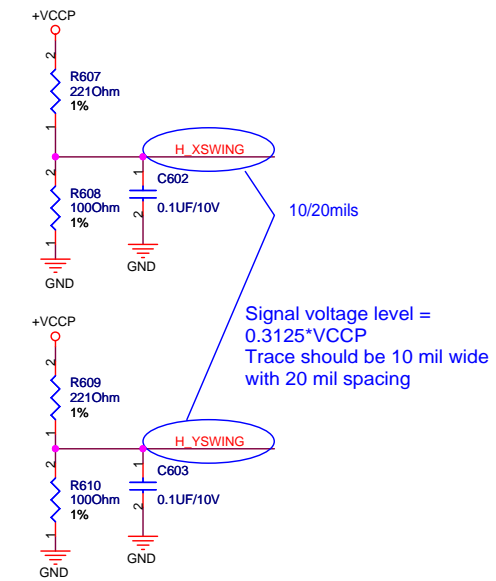
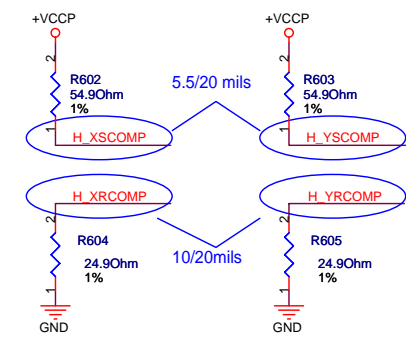
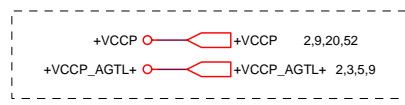
H_REQ#0	D8	H_REQ#0	
H_REQ#1	G8	H_REQ#1	
H_REQ#2	B8	H_REQ#2	
H_REQ#3	F8	H_REQ#3	
H_REQ#4	A8	H_REQ#4	

H_RS#0	B4	H_RS#0	
H_RS#1	E6	H_RS#1	
H_RS#2	D6	H_RS#2	

H_CPUSLP#	E3	H_CPUSLP#	2,17
H_TRDY#	E7	H_TRDY#	2



Layout Note:
0.1uF should be placed 100mils or less from GMCH pin.

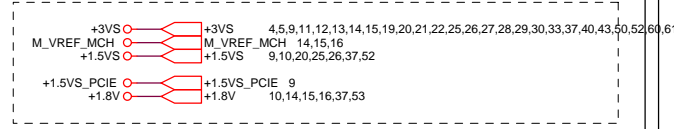
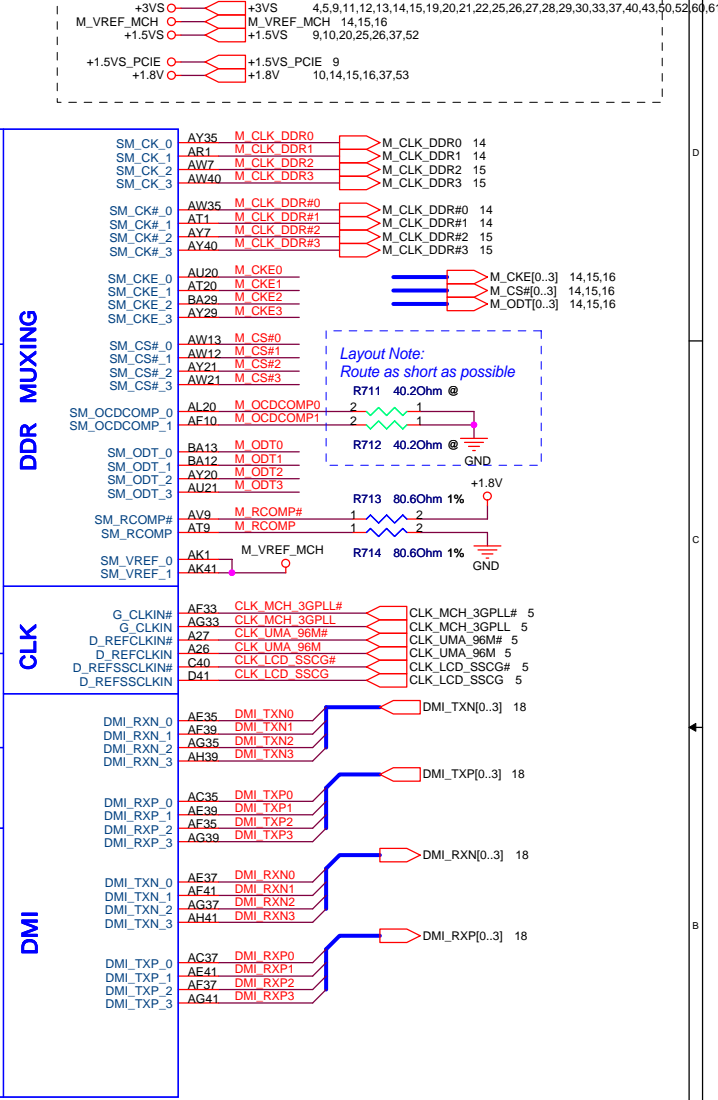
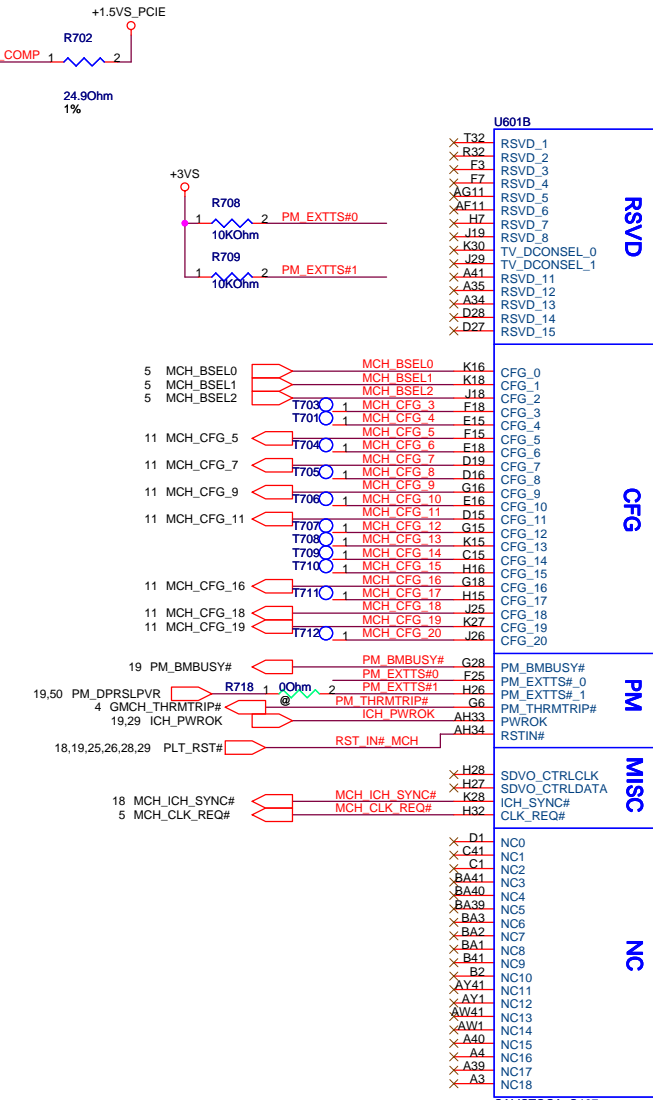
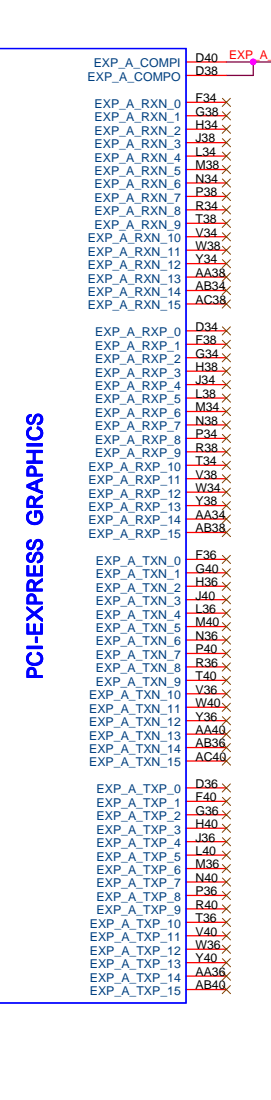
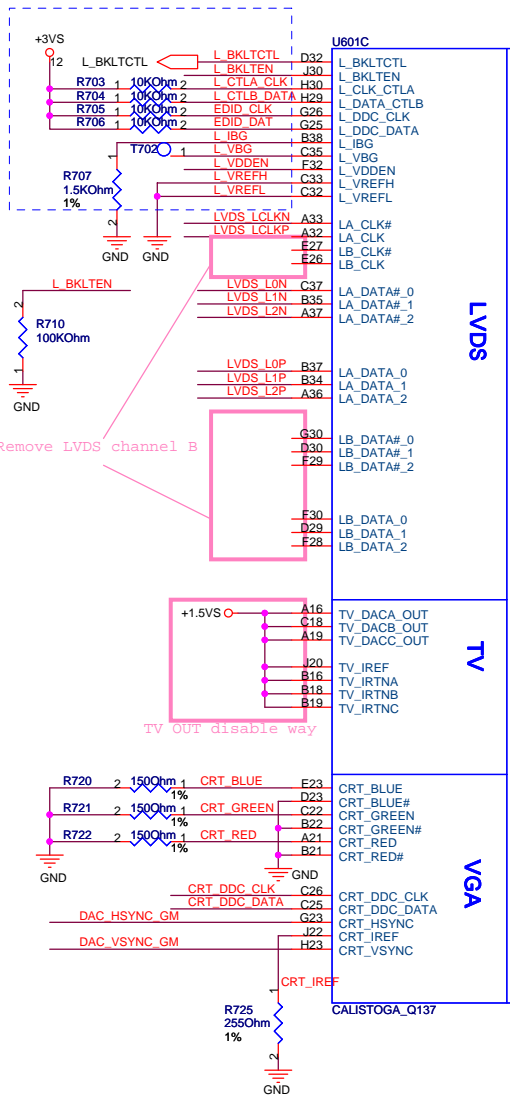


5 CLK_MCH_BCLK
5 CLK_MCH_BCLK#

H_XRCOMP E1 H_XRCOMP
H_XSCOMP E2 H_XSCOMP
H_XSWING E4 H_XSWING
H_YRCOMP Y1 H_YRCOMP
H_YSCOMP U1 H_YSCOMP
H_YSWING W1 H_YSWING

CALISTOGA_Q137

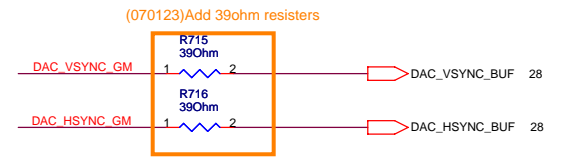
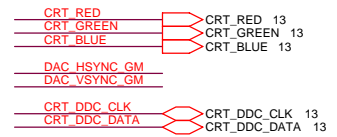
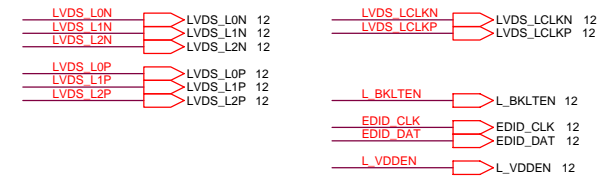
ASUS/ALPHA		Title : Calistoga GMCH (1)	
ASUSALPHATeK COMPUTER INC.		Engineer: Hong Chou	
Size	Project Name		Rev
Custom	TERESA		1.1
Date: Monday, February 05, 2007		Sheet	6 of 57

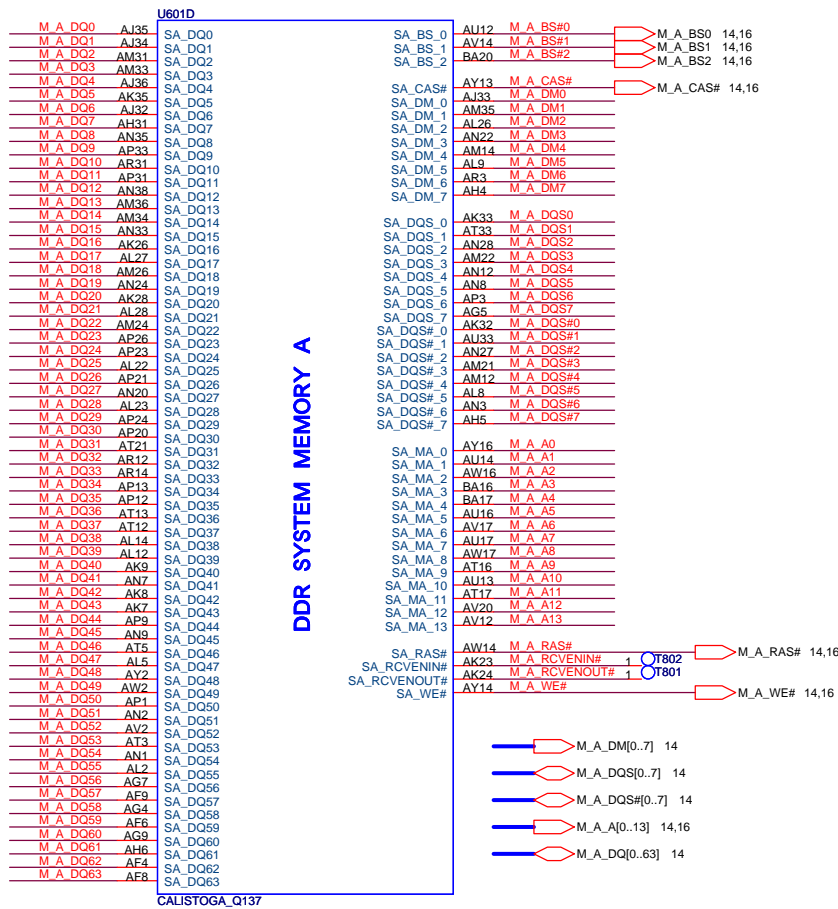


Layout Note:
Route as short as possible

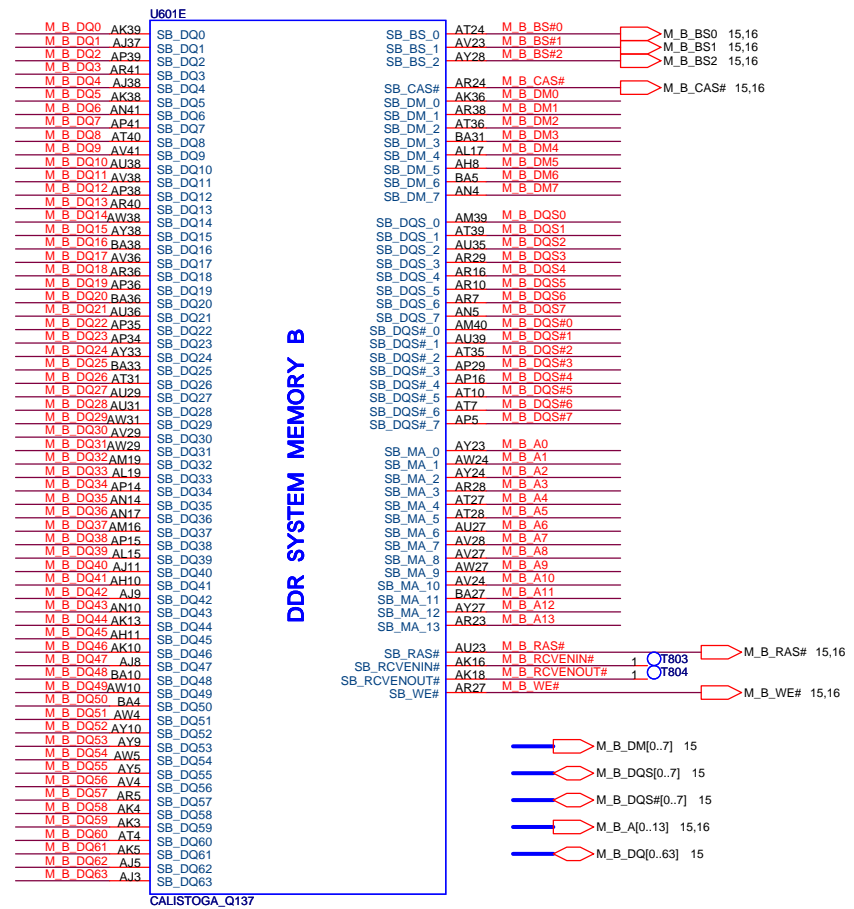
R711 40.2Ohm @

R712 40.2Ohm @

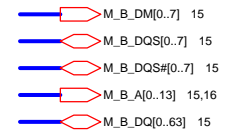




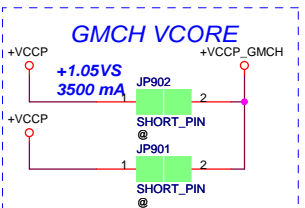
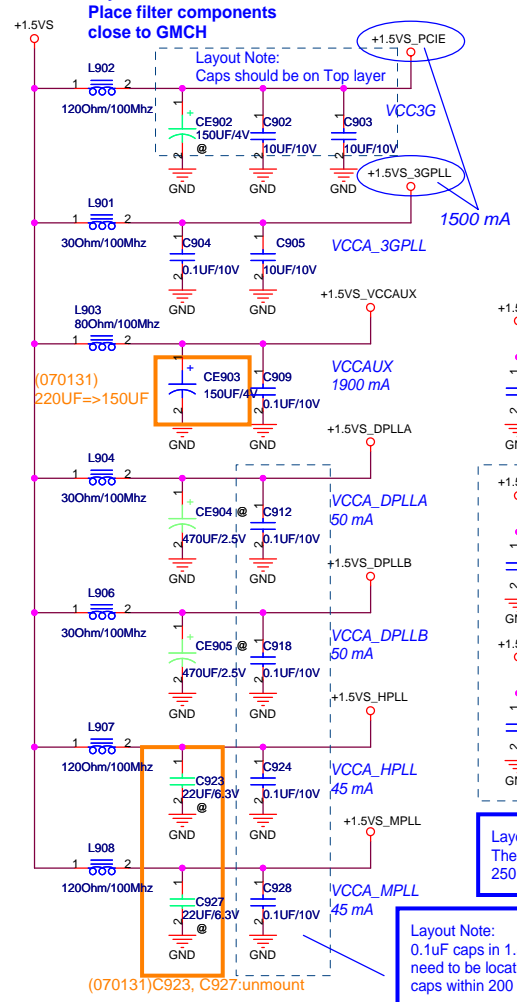
DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B



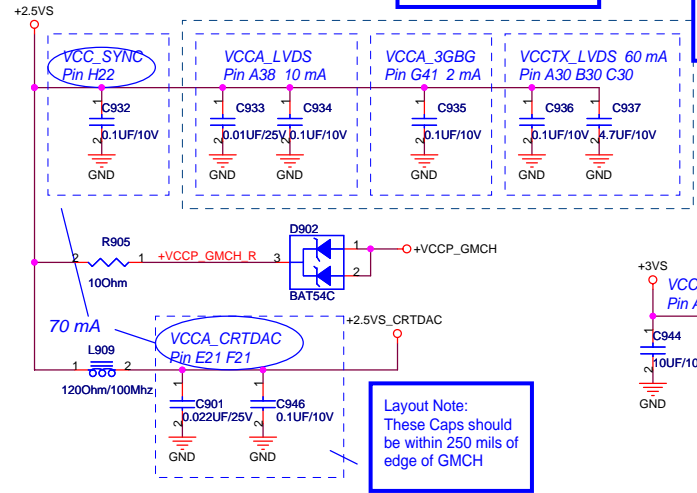
Layout Note:
Place filter components close to GMCH



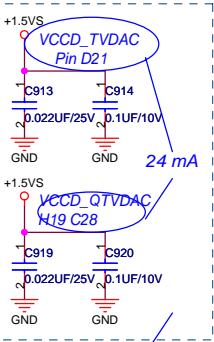
Layout Note:
These Caps should be within 250 mils of edge of GMCH

Layout Note:
0.1uF caps in 1.5V_xPLL need to be located as edge caps within 200 mils.

Layout Note:
These 0.1uF caps should be placed within 200 mils of edge



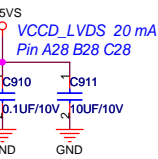
Layout Note:
These Caps should be within 250 mils of edge of GMCH



Layout Note:
These Caps should be within 250 mils of edge of GMCH

Layout Note:
These 0.1uF caps in 1.5V_xPLL need to be located as edge caps within 200 mils.

Layout Note:
These 0.1uF caps should be placed within 200 mils of edge



Layout Note:
These Caps should be within 250 mils of edge of GMCH

Layout Note:
These 0.1uF caps in 1.5V_xPLL need to be located as edge caps within 200 mils.

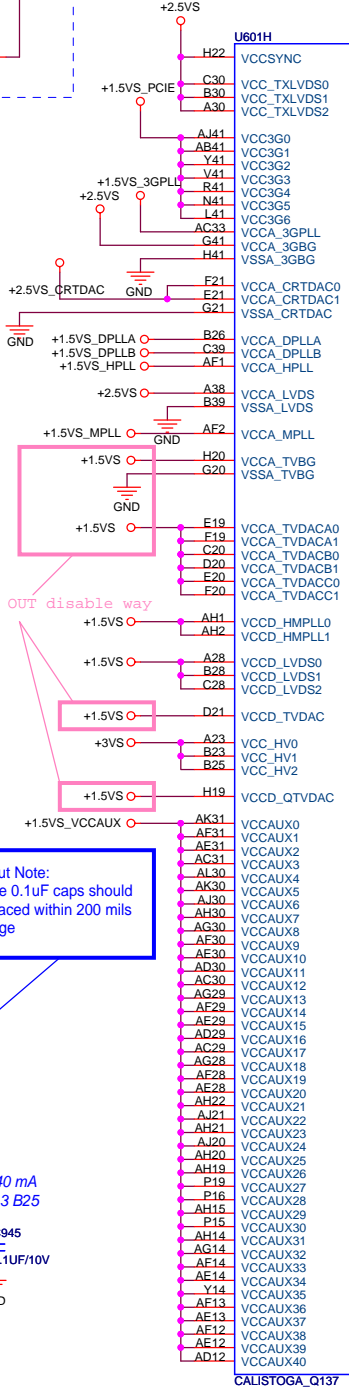
Layout Note:
These 0.1uF caps should be placed within 200 mils of edge

Layout Note:
These Caps should be within 250 mils of edge of GMCH

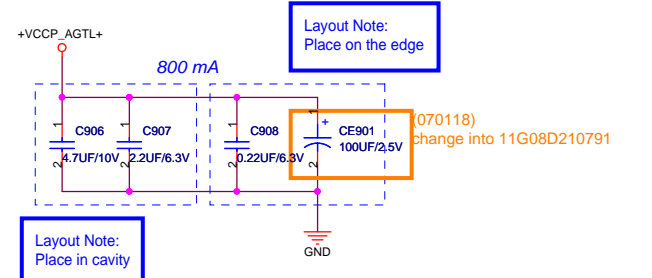
Layout Note:
These 0.1uF caps in 1.5V_xPLL need to be located as edge caps within 200 mils.

Layout Note:
These 0.1uF caps should be placed within 200 mils of edge

+VCCP_AGTL+	2,3,5,6
+VCCP_GMCH	10
+1.5V_S_PCIE	7
+3VS	4,5,7,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,40,43,50,52,60,61
+2.5VS	37,54
+1.5VS	7,10,20,25,26,37,52



POWER



Layout Note:
Place in cavity

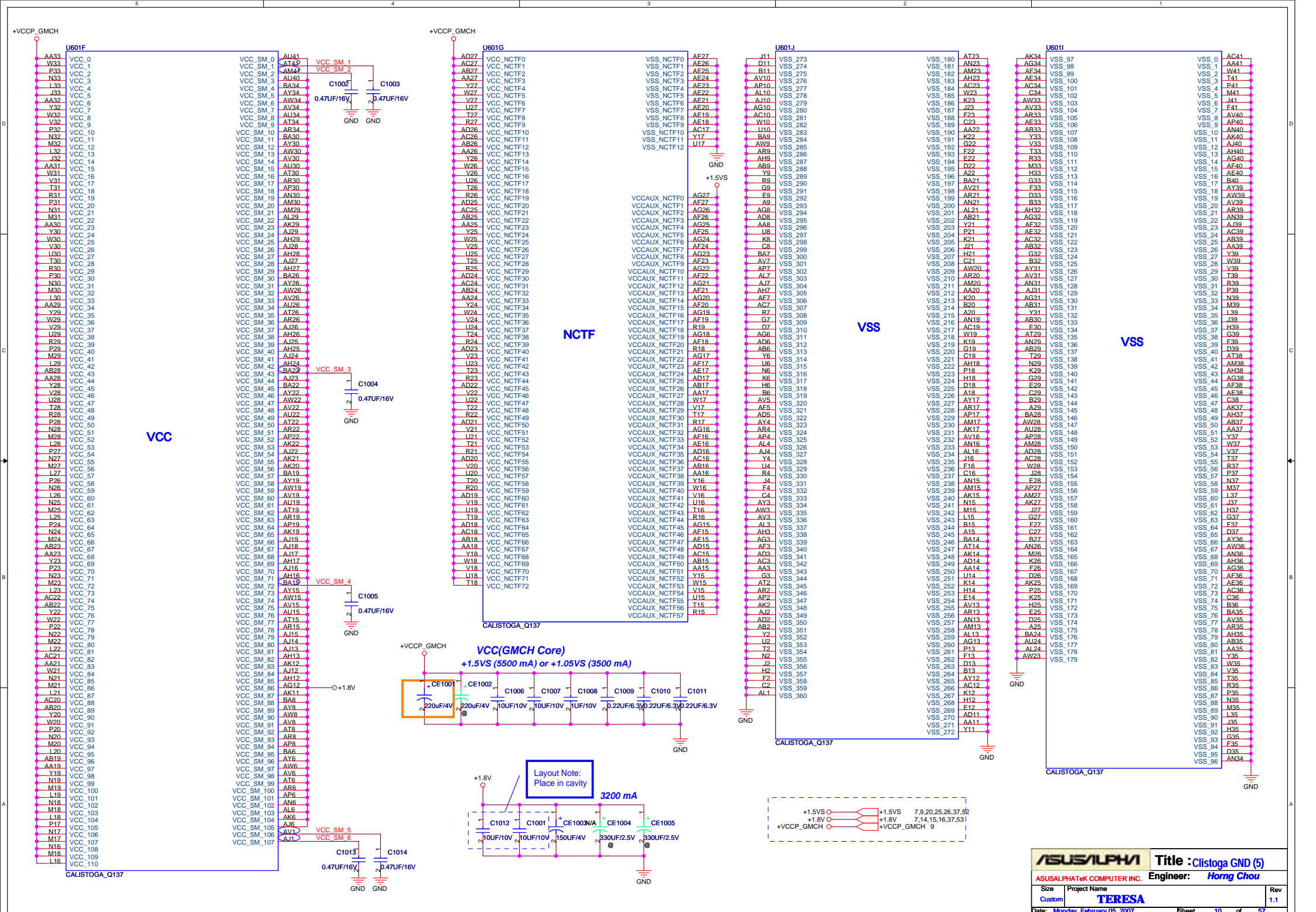
Layout Note:
Place on the edge

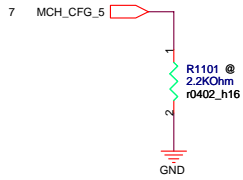


Remove TV OUT Power

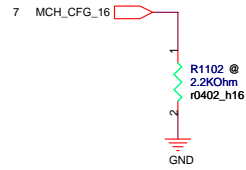
NOTE: 0.1UF CAPS USED IN +1.5V, +3.3VS +2.5VS should be placed within 200 mils of edge.

ASUS ALPHA		Title : Calistoga Power (4)	
ASUSALPHA@K COMPUTER INC.		Engineer: Horng Chou	
Size	Project Name	Rev	1.1
Custom	TERESA	Date:	Monday, February 05, 2007
Sheet		9	of 57

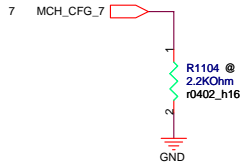




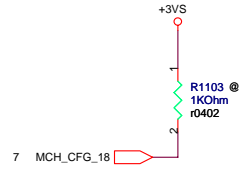
CFG5 : DMI X2 Select
 LOW = DMI X 2
HIGH = DMI X 4 (Default)



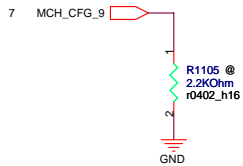
CFG16 : FSB DYNAMIC ODT
 LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



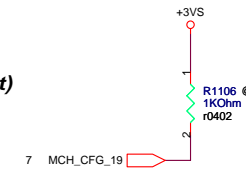
CFG7 : CPU STRAP
 LOW = Reserved
HIGH = Mobility CPU (Default)



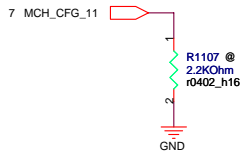
CFG18 : GMCH Core Voltage Level
 LOW = 1.05V
HIGH = 1.5V (default)



CFG9 : PCIE GRAPHIC LANE
 LOW = REVERSE LANES
HIGH = NORMAL OPERATION (Default)



CFG19 : DMI LANE REVERSAL
 LOW = NORMAL
 HIGH = LANES REVERSED



CFG11 : Reserved but need to be pull low

CFG[17..3] have internal pullup resistors.
 CFG[19..18] have internal pulldown resistors.
 SDVOCRTL_DATA has internal pulldown resistors.

CFG All are sampled with respect to the leading edge of the GMCH PWROK

2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_C TRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

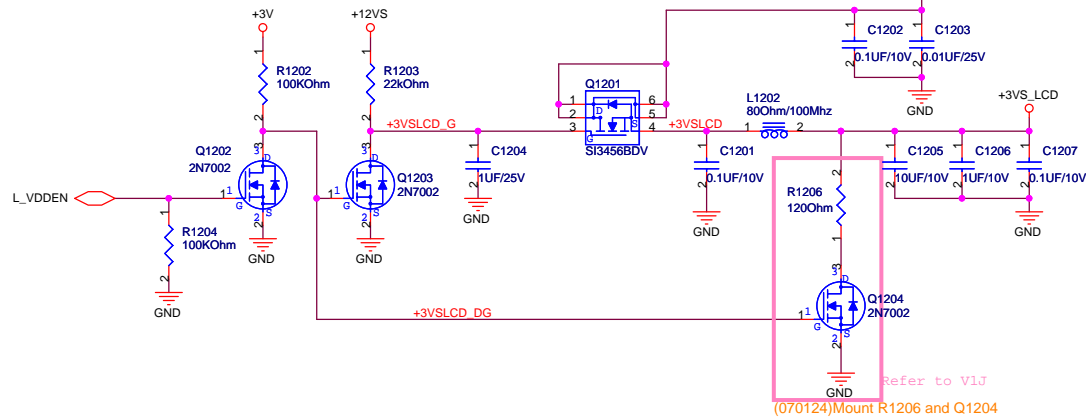
(061215)Remove +2.5VS power supply



LCD Panel Power

3~3.6V
Full Active: 410 mA(Max. 500 mA)
3~3.6V
S0-S1 M: 410 mA(Max. 500 mA)

Remove CMOS Camera(USB4)

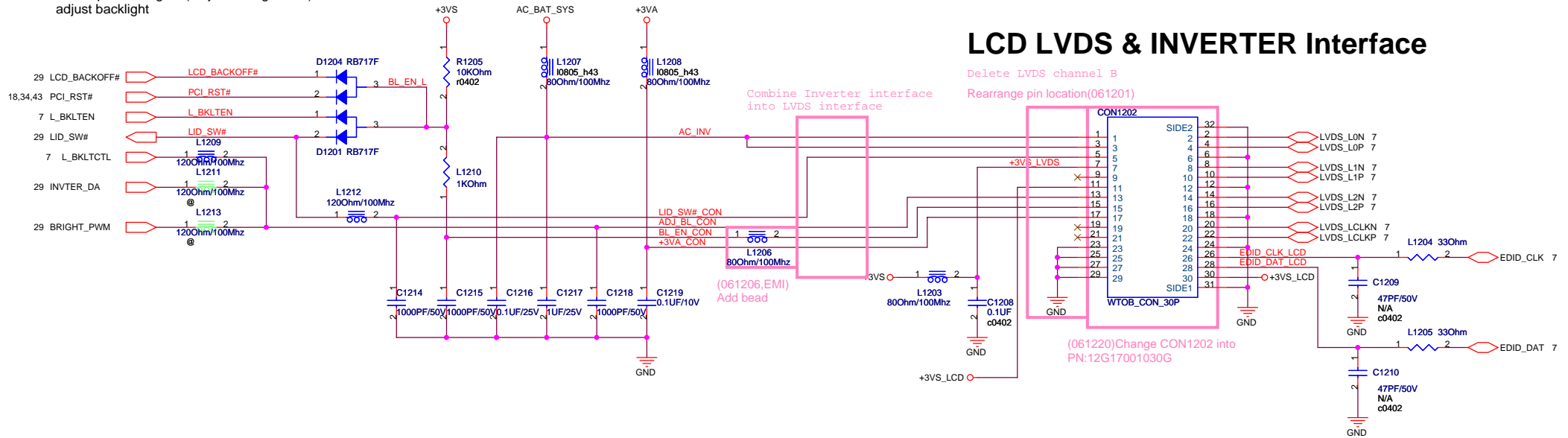


LCD Backlight Control

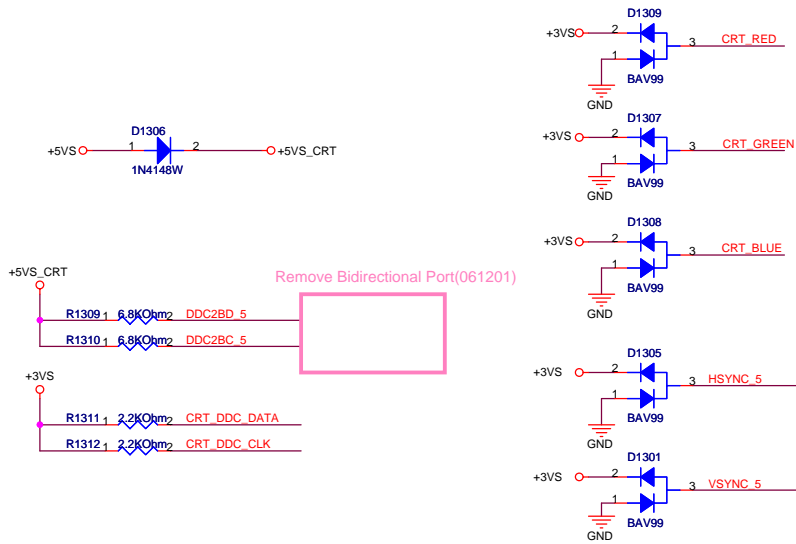
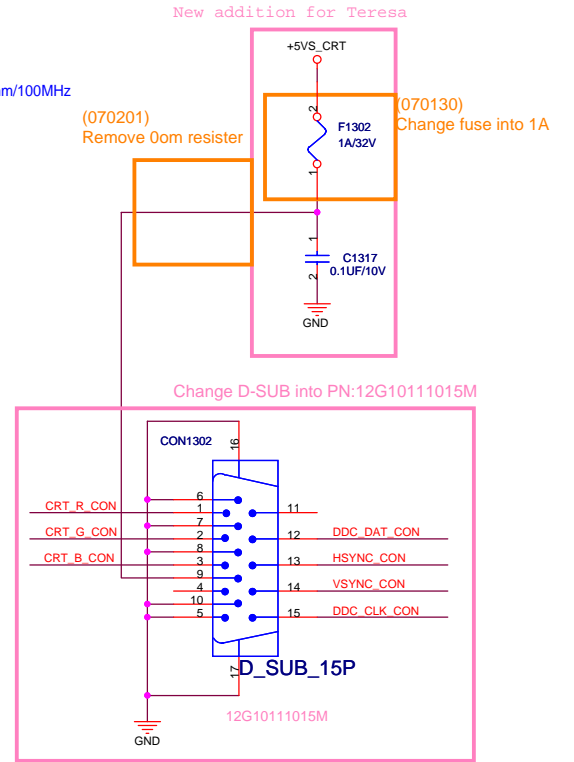
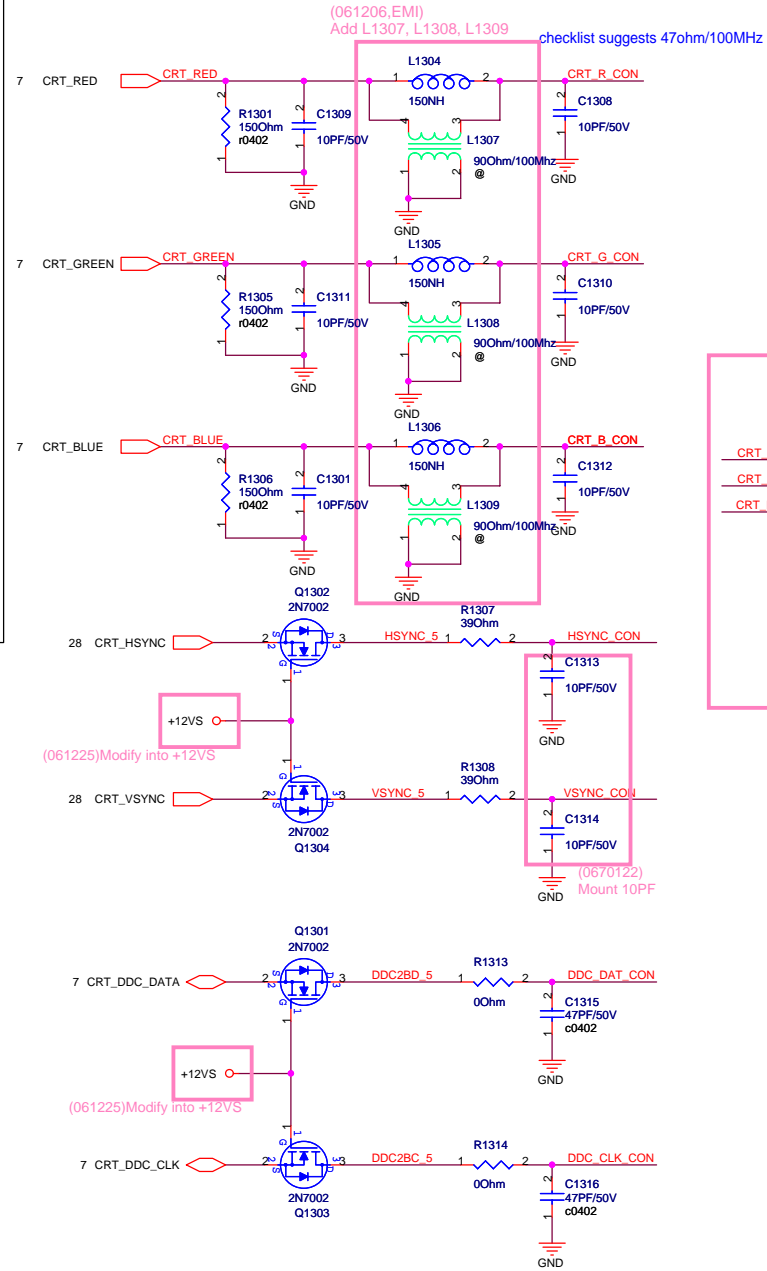
BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to
adjust backlight

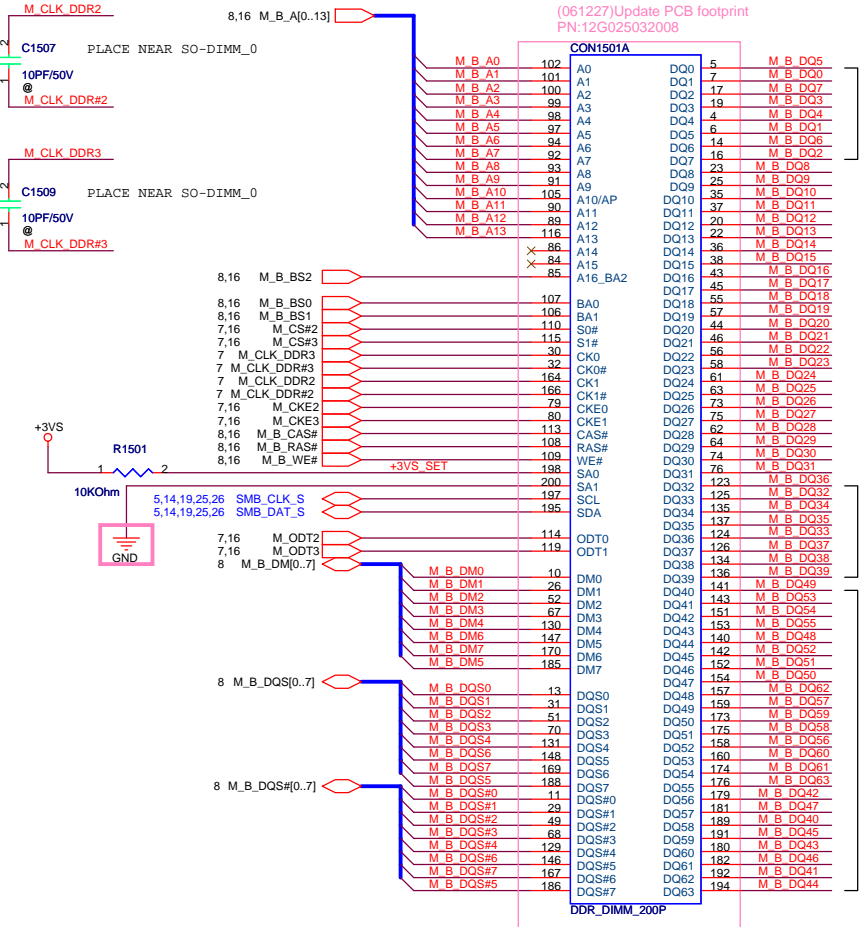
**Inverter Board
built in 15.4W
LCD Panel**



CRT OUT

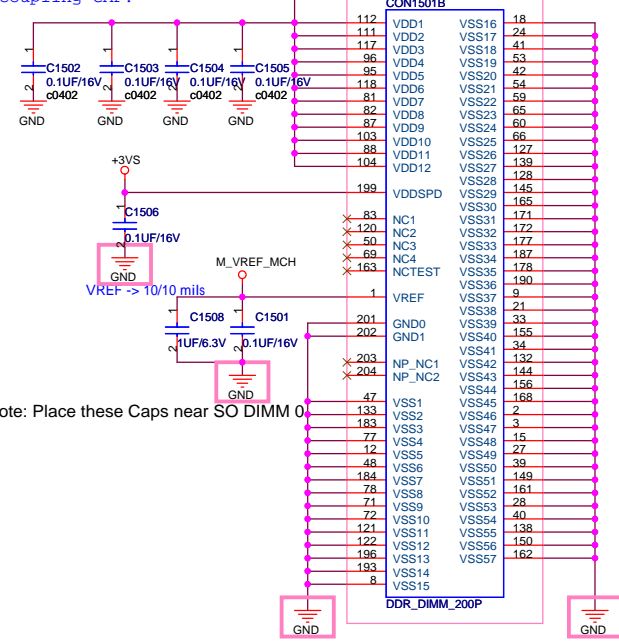


SMBus Slave Address:A4H

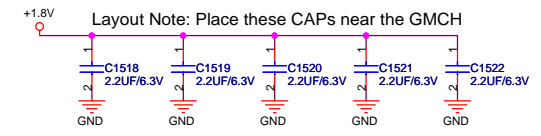
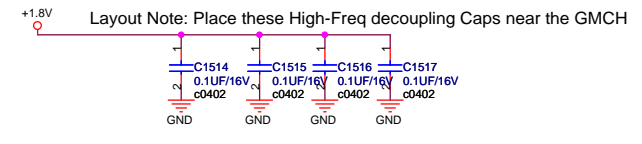
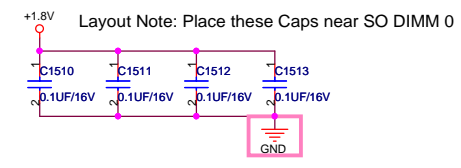


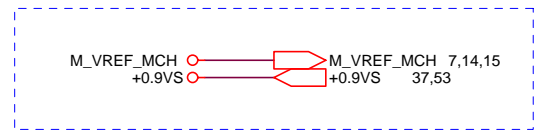
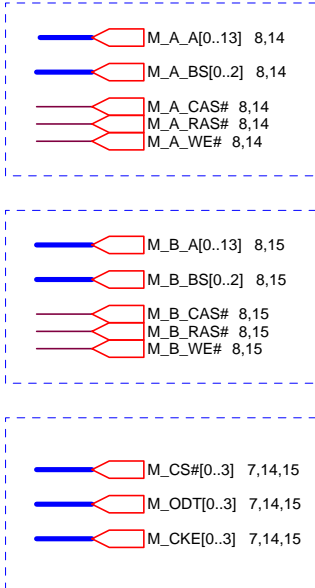
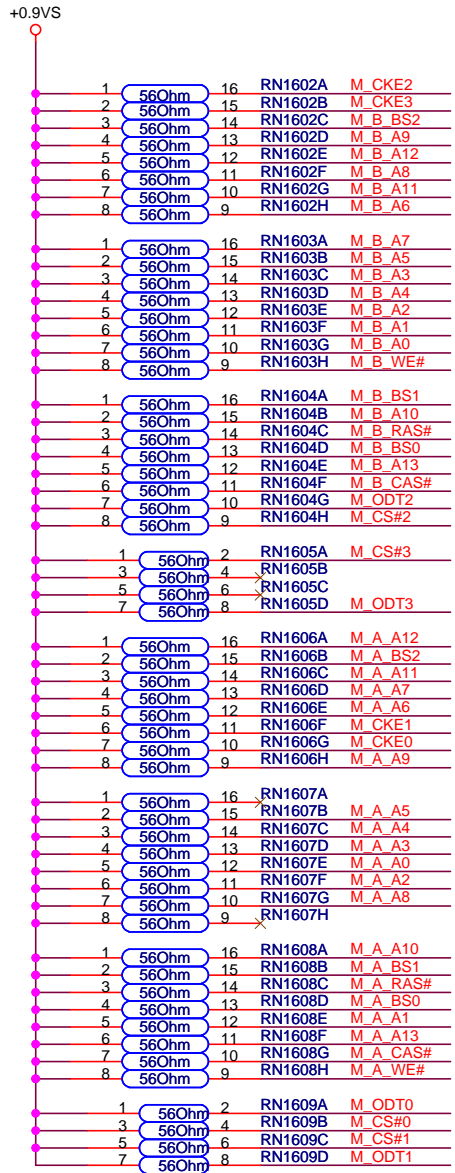
Address reference +1.8V, add four 0.1uF decoupling CAP.

(061227)Update PCB footprint
PN:12G025032008

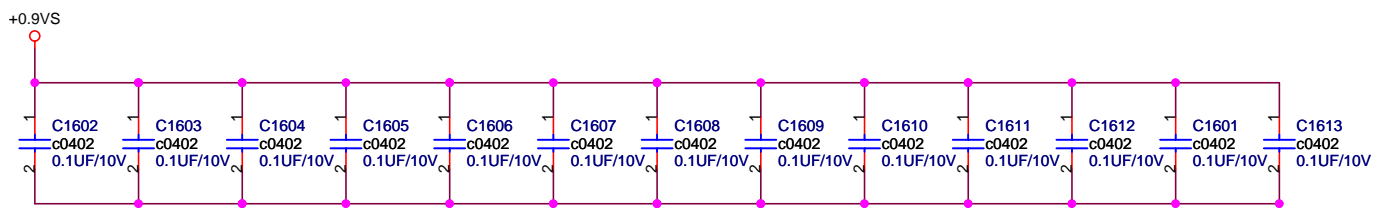
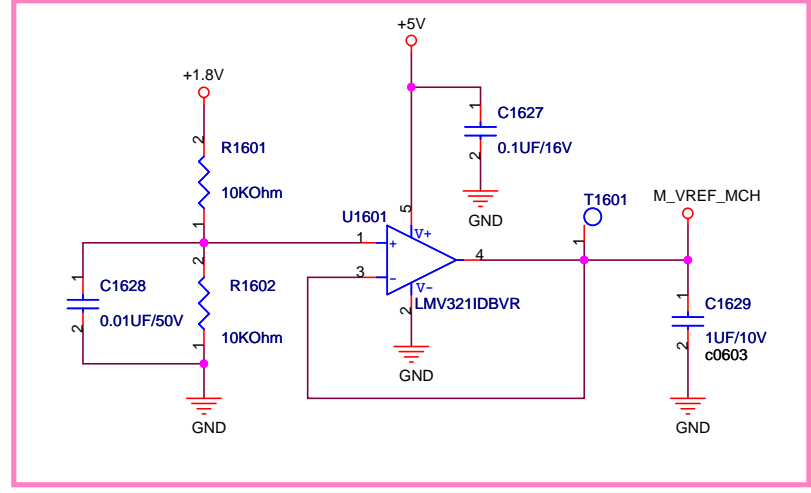


Layout Note: Place these Caps near SO DIMM 0

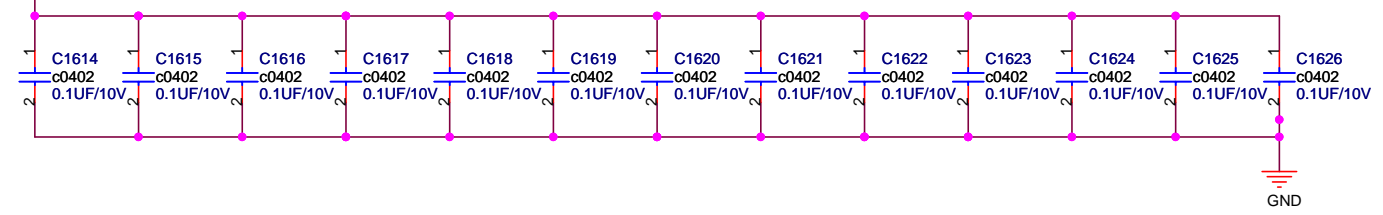


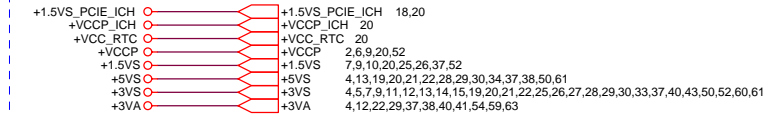
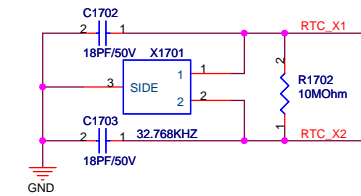
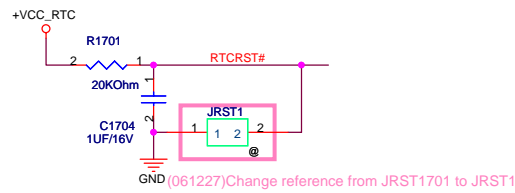


Add Voltage Follower

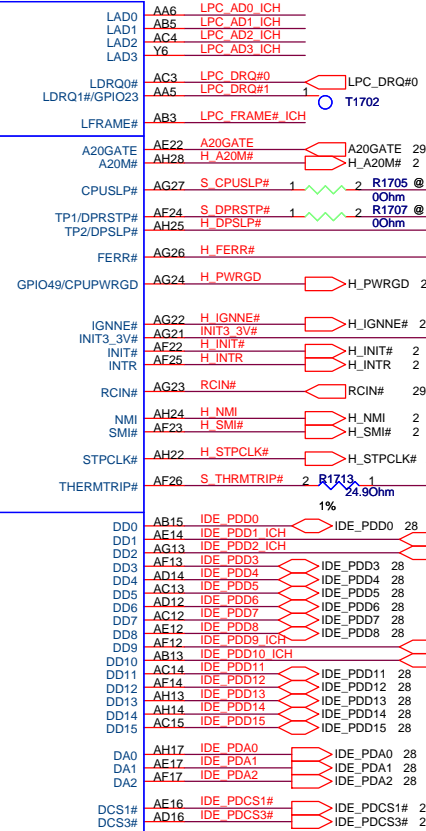
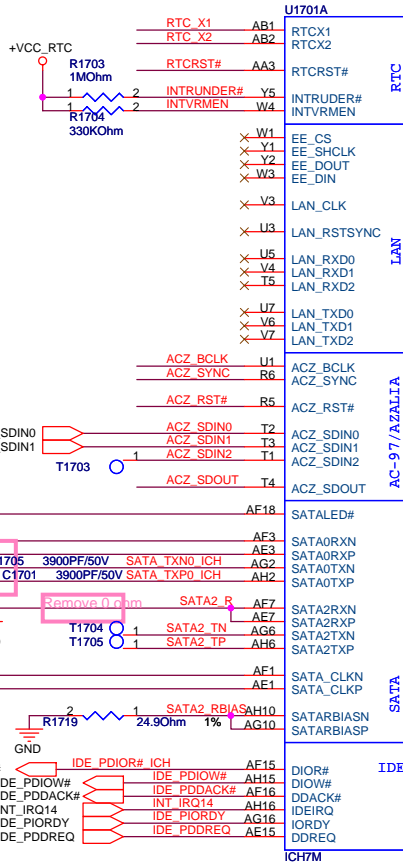
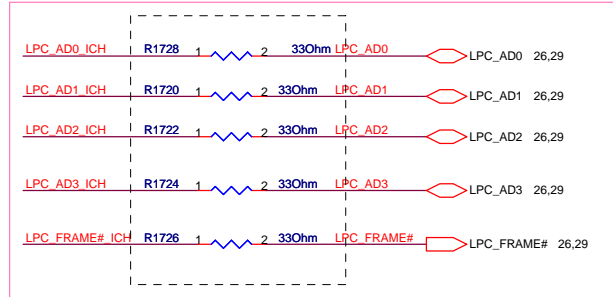


Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS



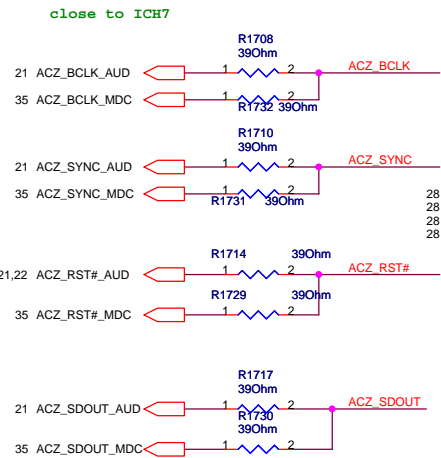


Delete LPC interface of TPM



DPRSTP# routing from Intel 82801GBM to Yonah processor is required. Routing to VR must be done last and must have de-bounce filtering to handle daisy chain topology.

24 ± 5% series termination resistor placed within 2" from Intel 82801GBM, 56 ± 5% pull-up resistor has to be within 2" from the series resistor



Change to 3900PF, Remove 0.0Ohm

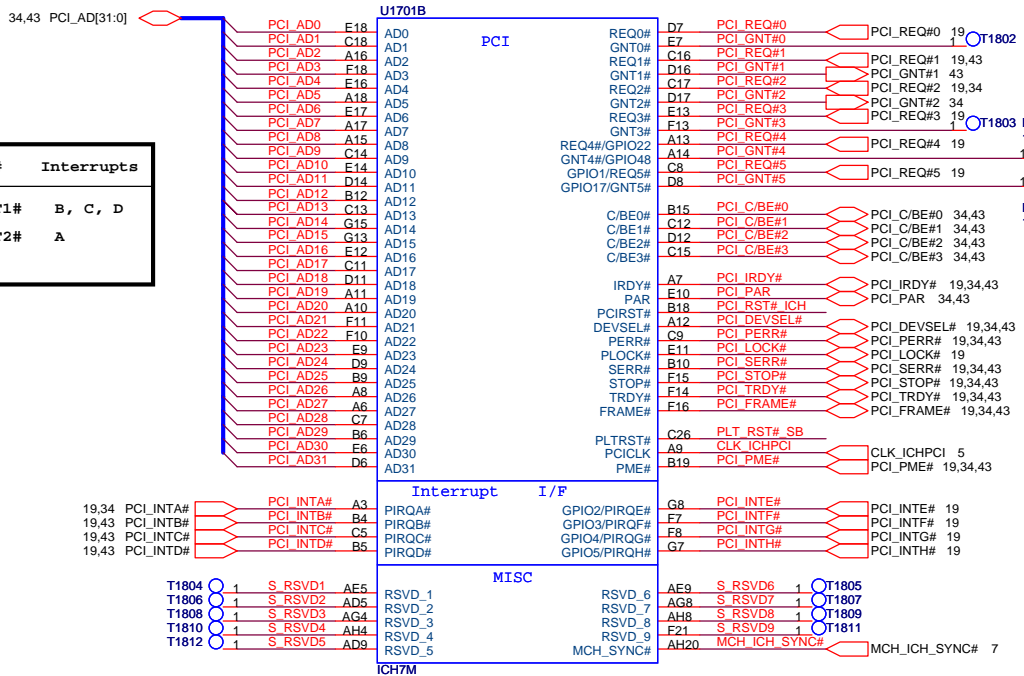
Check with EMI: remove 0 ohm => IDE_PDIOIR#_ICH, IDE_PDD1_ICH, IDE_PDD2_ICH, IDE_PDD9_ICH, IDE_PDD10_ICH

ACZ_SDOUT	PWROK rising	TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC	PD
ACZ_SYNC	PWROK rising	sets bit 0 of RPC.PC	PD
EE_CS		should not be pulled high	PD
EE_DOUT		should not be pulled low	PU
GNT2#		should not be pulled low	PU
GNT3#	PWROK rising	low: "top-block swap" mode	PU
GNT5#/GPIO17# GNT4#/GPIO48	PWROK rising	GNT5# GNT4# 0 1 SPI 1 0 PCI 1 1 LPC	PU

GPIO16 /DPRSLPVR		should not be pulled high	PD
GPIO25	RSRST# rising	should not be pulled low	PU
INTRVREN	ALWAYS	high: Enable integrated VccSus1_05 VRM	
LINKALER#		REQUIRE an external pull-up R	Need PU
RBQ[4:1]#	PWROK rising		
SATALED#		should not be pulled low	Conditional PU
SPKR	PWROK rising	high: "No reboot" mode	PD
TP3	PWROK rising	should not be pulled low unless using XOR Chain testing	PU

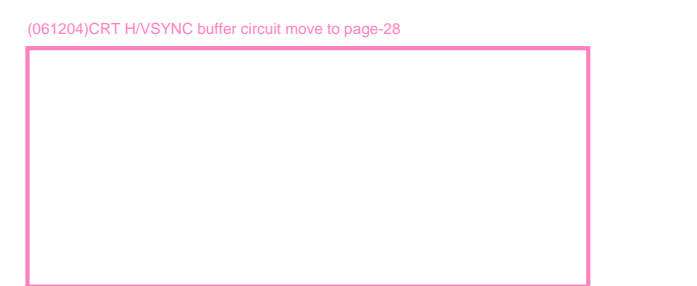
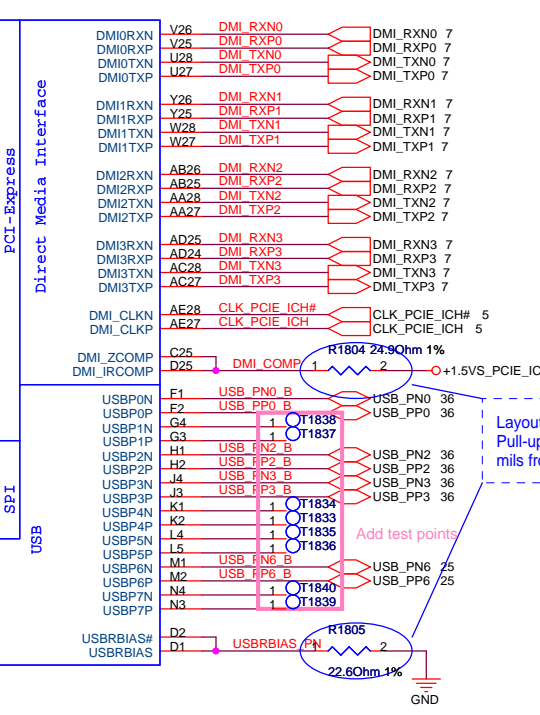
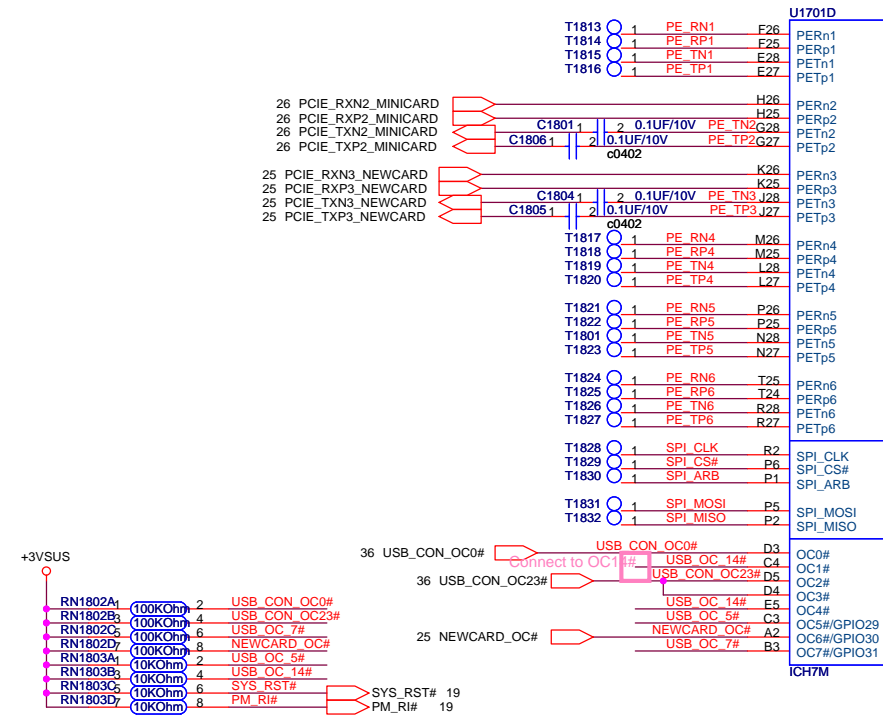
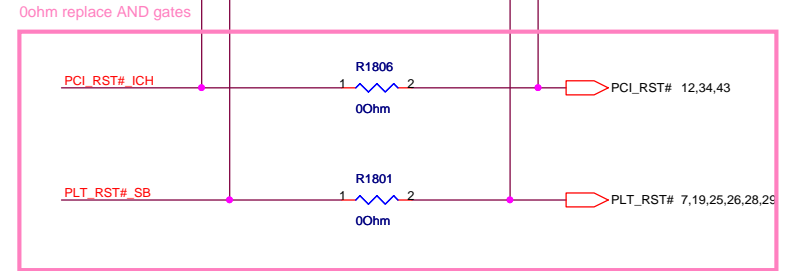
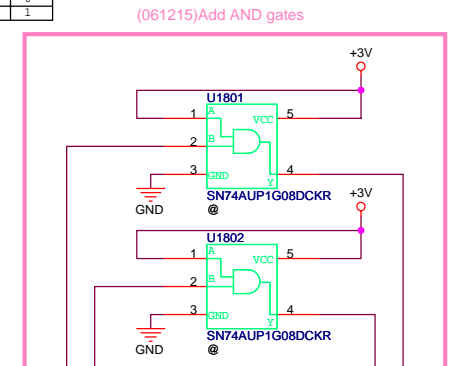
PCI Device

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A



	GNT#5	GNT#4
LPC	1	1
PCI	1	0
SPI	0	1

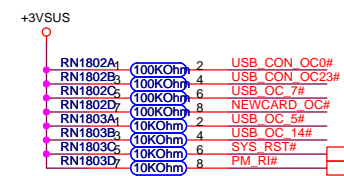
(default)

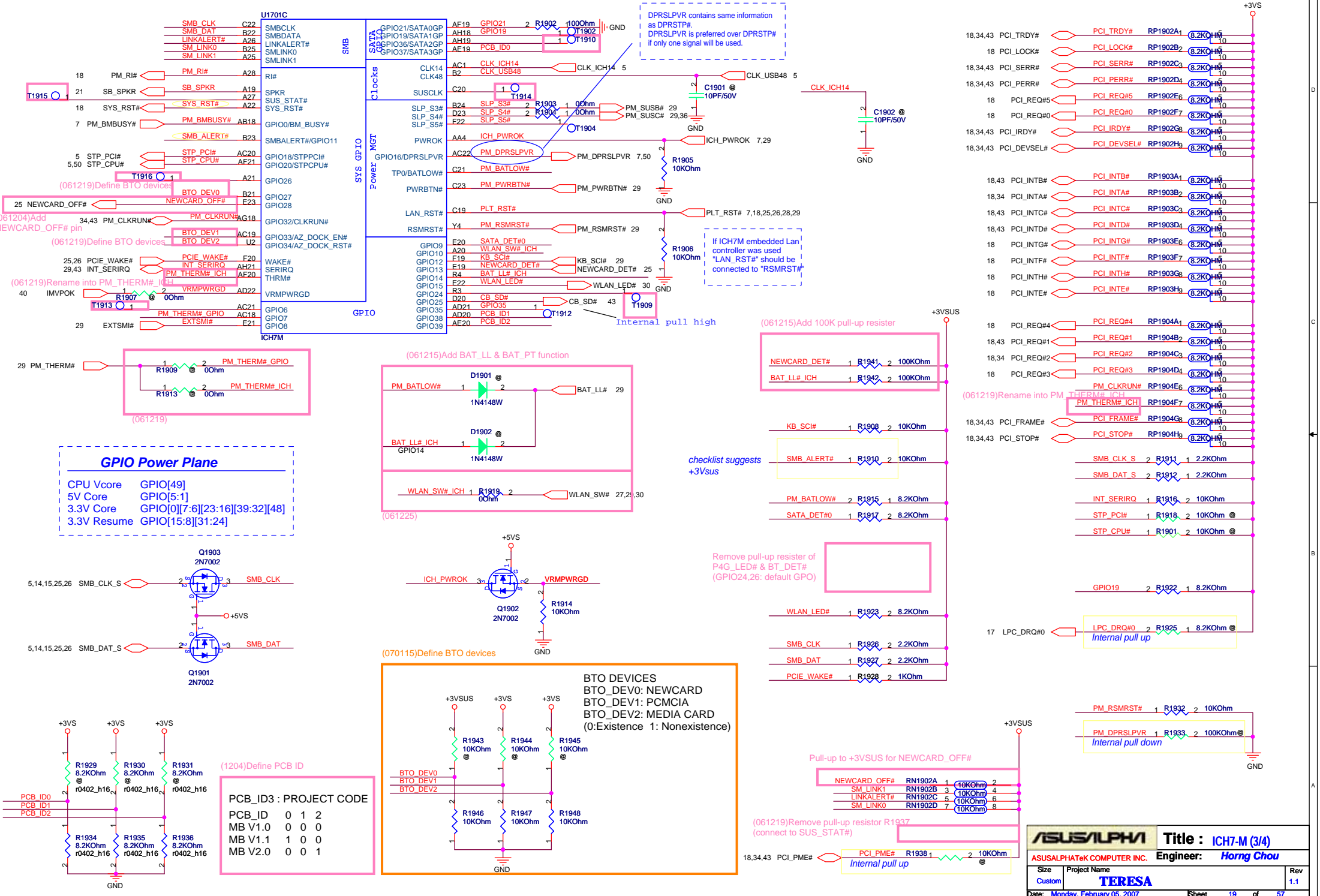


Modify USB Device table

USB Devices	
Port 0	CON3602
Port 1	Unused
Port 2	CON3601
Port 3	CON3601
Port 4	Unused
Port 5	Unused
Port 6	NewCard
Port 7	Unused

Layout Note:
Pull-ups must be placed within 500 mils from Intel 82801GBM pins





DPRSLPVR contains same information as DPRSTP#. DPRSLPVR is preferred over DPRSTP# if only one signal will be used.

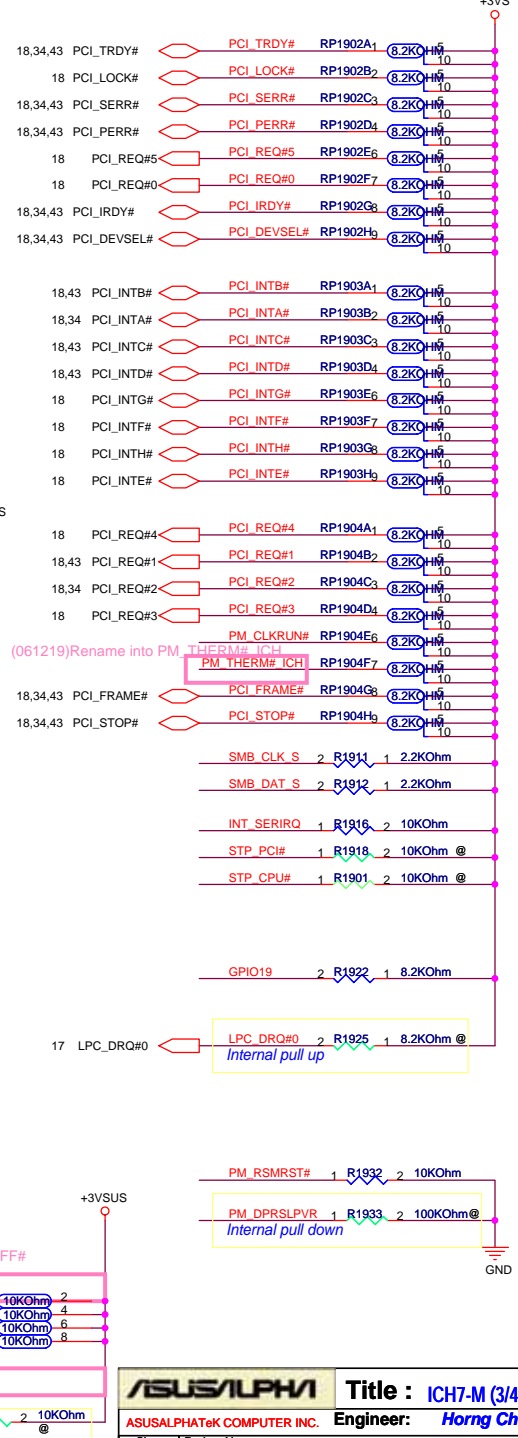
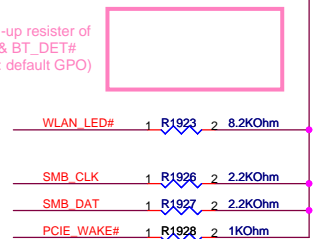
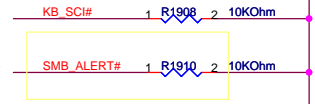
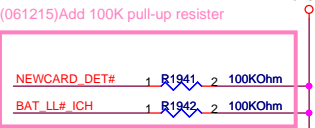
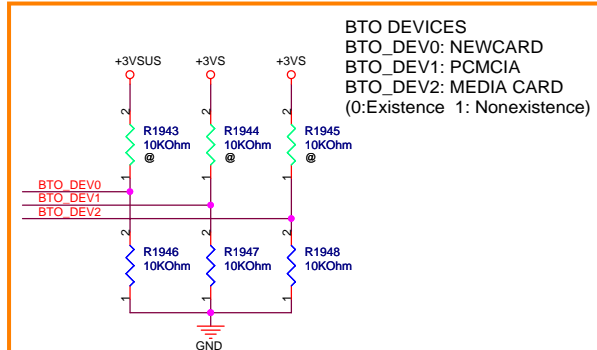
If ICH7M embedded Lan controller was used "LAN_RST#" should be connected to "RSMRST#"

GPIO Power Plane

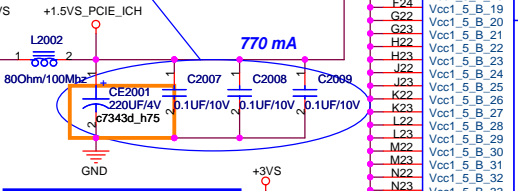
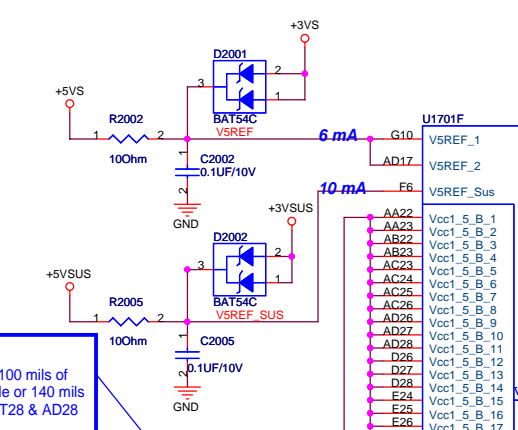
CPU Vcore GPIO[49]
 5V Core GPIO[5:1]
 3.3V Core GPIO[0][7:6][23:16][39:32][48]
 3.3V Resume GPIO[15:8][31:24]

(1204) Define PCB ID

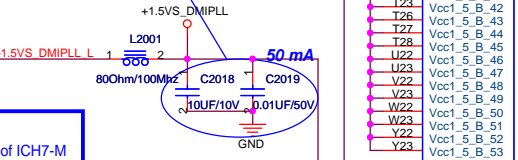
PCB_ID3 : PROJECT CODE	0	1	2
MB V1.0	0	0	0
MB V1.1	1	0	0
MB V2.0	0	0	1



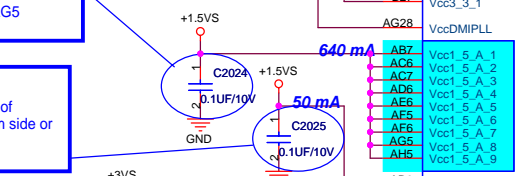
Layout Note:
Place above Caps within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin D28, T28 & AD28



Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top

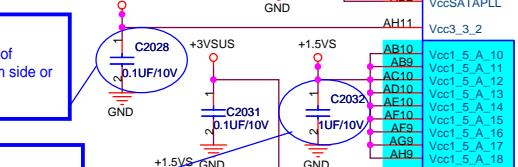


Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG5

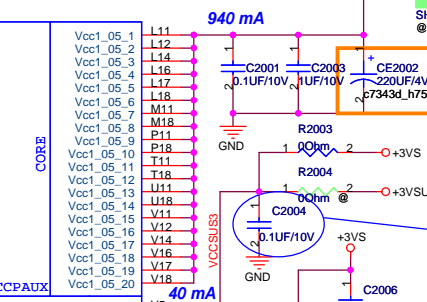
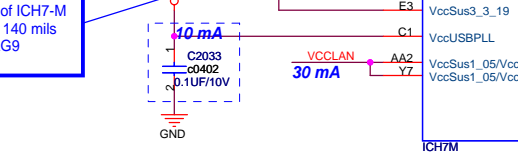


Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top

Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top

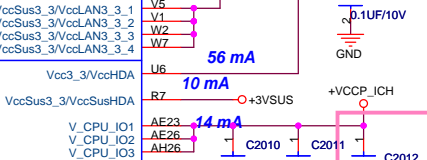


Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG9



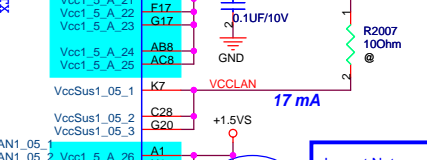
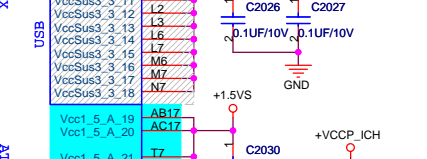
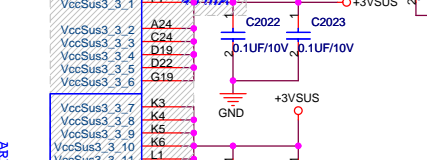
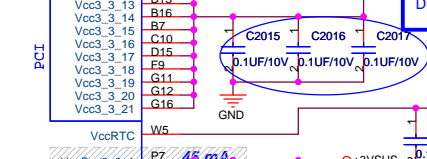
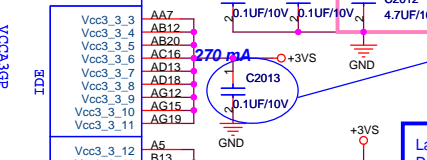
If ICH7 embedded Lan controller was used, these pins should connect to +3VSUS for S3-S5 wake up.

Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin

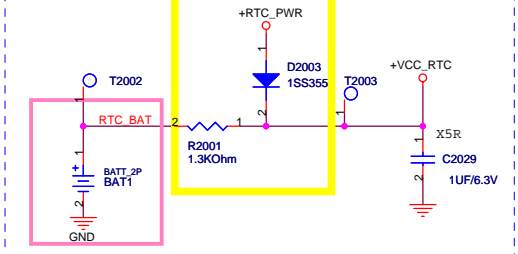


Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin

Layout Note:
Distribute in PCI section



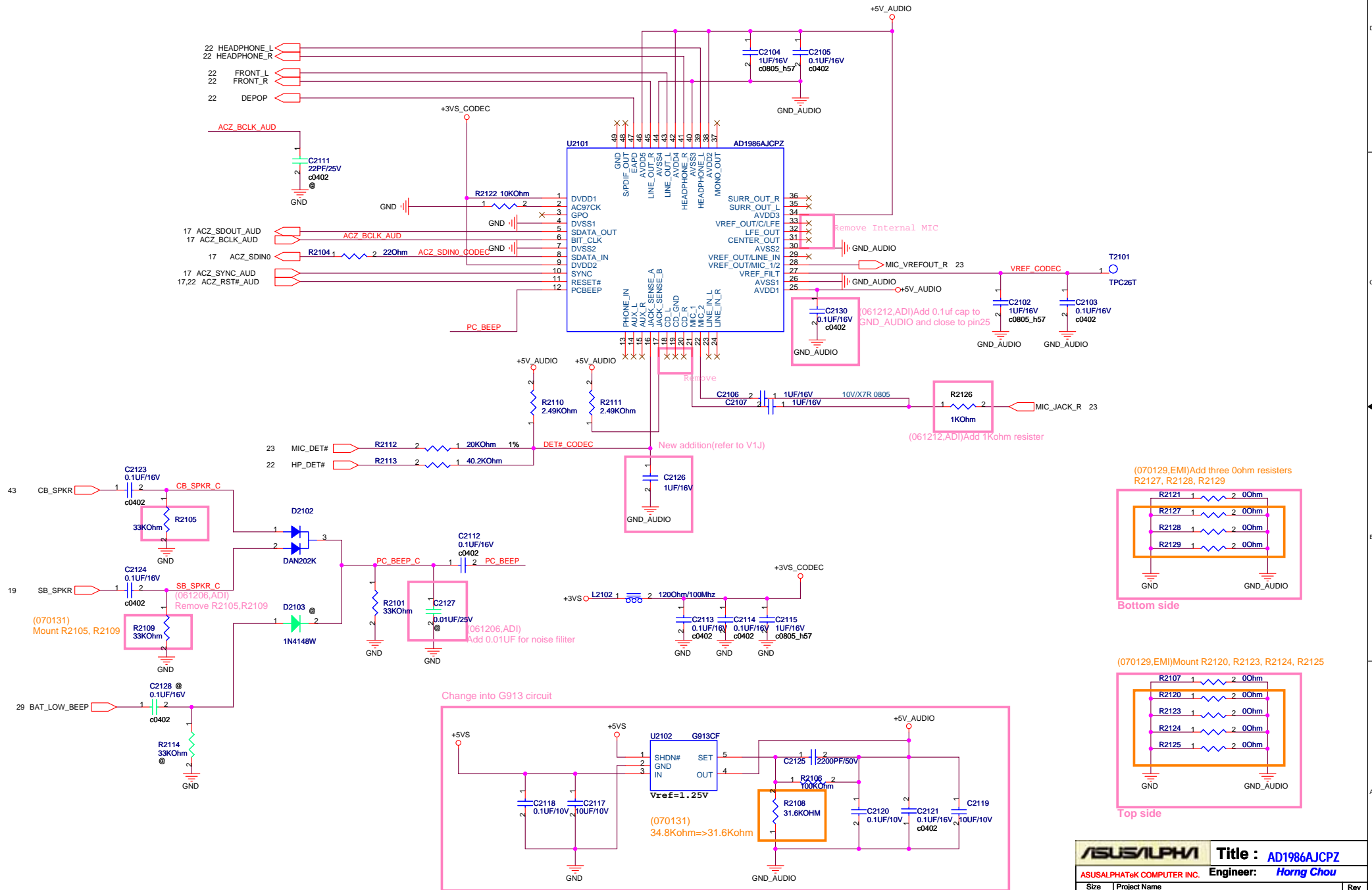
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top

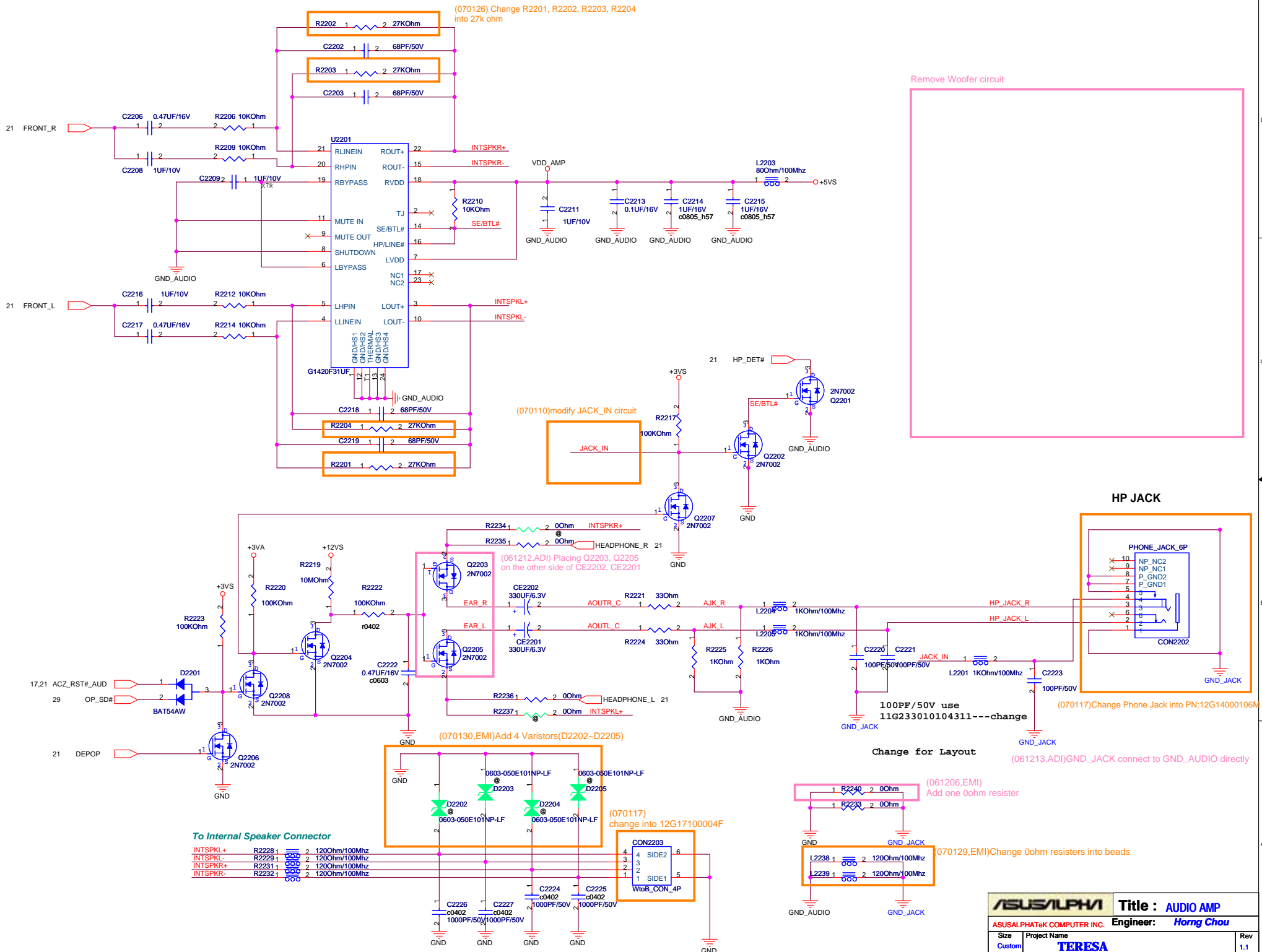


(1204)Change battery into rechargeable type (PN:07G016021220) PANASONIC ML1220-F1BE 07G016021220 MAXELL ML1220T10 07G016031220

(061207.Power) Modify for RTC charge circuit

U1701E		
A4	Vss1	P28
A23	Vss2	R1
B1	Vss3	Vss99
B8	Vss4	Vss100
B11	Vss5	Vss101
B14	Vss6	Vss102
B17	Vss7	Vss103
B20	Vss8	Vss104
B28	Vss9	Vss105
C2	Vss10	Vss106
C6	Vss11	Vss107
D10	Vss12	Vss108
D17	Vss13	Vss109
D18	Vss14	Vss110
D21	Vss15	Vss111
D24	Vss16	Vss112
E1	Vss17	Vss113
E2	Vss18	Vss114
E4	Vss19	Vss115
E8	Vss20	Vss116
F4	Vss21	Vss117
F8	Vss22	Vss118
F15	Vss23	Vss119
F22	Vss24	Vss120
F28	Vss25	Vss121
G1	Vss26	Vss122
G2	Vss27	Vss123
G3	Vss28	Vss124
G6	Vss29	Vss125
G9	Vss30	Vss126
G14	Vss31	Vss127
G18	Vss32	Vss128
G21	Vss33	Vss129
G25	Vss34	Vss130
G26	Vss35	Vss131
H3	Vss36	Vss132
H4	Vss37	Vss133
H5	Vss38	Vss134
H24	Vss39	Vss135
H27	Vss40	Vss136
H28	Vss41	Vss137
J1	Vss42	Vss138
J2	Vss43	Vss139
J5	Vss44	Vss140
J24	Vss45	Vss141
J25	Vss46	Vss142
K26	Vss47	Vss143
K27	Vss48	Vss144
K28	Vss49	Vss145
L13	Vss50	Vss146
L15	Vss51	Vss147
L24	Vss52	Vss148
L25	Vss53	Vss149
L26	Vss54	Vss150
M3	Vss55	Vss151
M4	Vss56	Vss152
M5	Vss57	Vss153
M12	Vss58	Vss154
M13	Vss59	Vss155
M14	Vss60	Vss156
M15	Vss61	Vss157
M16	Vss62	Vss158
M17	Vss63	Vss159
M27	Vss64	Vss160
M28	Vss65	Vss161
N1	Vss66	Vss162
N2	Vss67	Vss163
N6	Vss68	Vss164
N5	Vss69	Vss165
N6	Vss70	Vss166
N11	Vss71	Vss167
N12	Vss72	Vss168
N13	Vss73	Vss169
N14	Vss74	Vss170
N15	Vss75	Vss171
N16	Vss76	Vss172
N17	Vss77	Vss173
N18	Vss78	Vss174
N19	Vss79	Vss175
N24	Vss80	Vss176
N25	Vss81	Vss177
N3	Vss82	Vss178
N4	Vss83	Vss179
N5	Vss84	Vss180
N6	Vss85	Vss181
N7	Vss86	Vss182
N8	Vss87	Vss183
N9	Vss88	Vss184
P4	Vss89	Vss185
P12	Vss90	Vss186
P13	Vss91	Vss187
P14	Vss92	Vss188
P15	Vss93	Vss189
P16	Vss94	Vss190
P17	Vss95	Vss191
P24	Vss96	Vss192
P27	Vss97	Vss193
	Vss98	Vss194
	Vss99	
	Vss100	
	Vss101	
	Vss102	
	Vss103	
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	Vss160	
	Vss161	
	Vss162	
	Vss163	
	Vss164	
	Vss165	
	Vss166	
	Vss167	
	Vss168	
	Vss169	
	Vss170	
	Vss171	
	Vss172	
	Vss173	
	Vss174	
	Vss175	
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	Vss178	
	Vss179	
	Vss180	
	Vss181	
	Vss182	
	Vss183	
	Vss184	
	Vss185	
	Vss186	
	Vss187	
	Vss188	
	Vss189	
	Vss190	
	Vss191	
	Vss192	
	Vss193	
	Vss194	





To Internal Speaker Connector

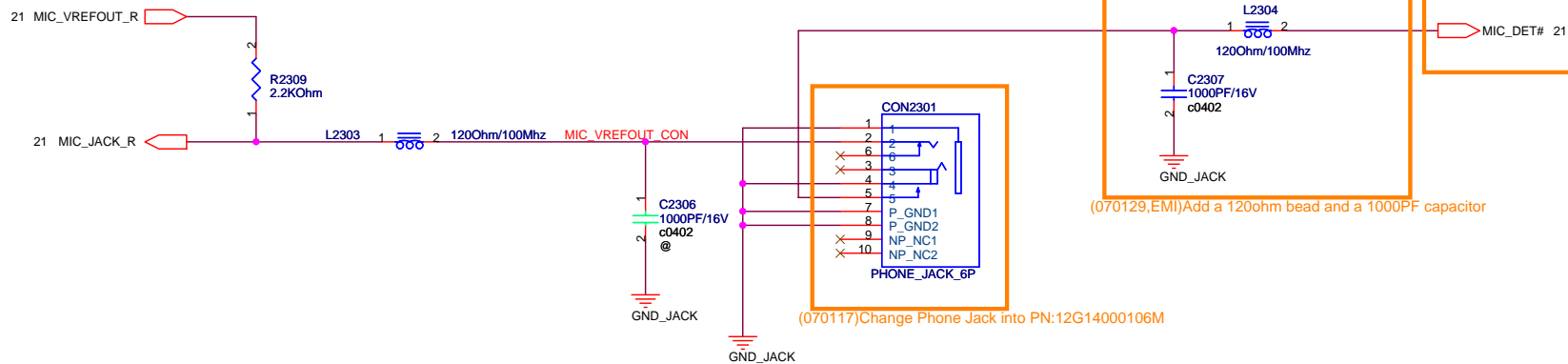
INTSPKL+	R2228	1	2	120Ohm/100Mhz
INTSPKL-	R2229	1	2	120Ohm/100Mhz
INTSPKR+	R2231	1	2	120Ohm/100Mhz
INTSPKR-	R2232	1	2	120Ohm/100Mhz

Remove Internal MIC pre-Amplifier

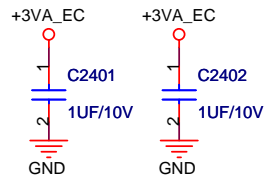


(070110)modify MIC_DET# circuit

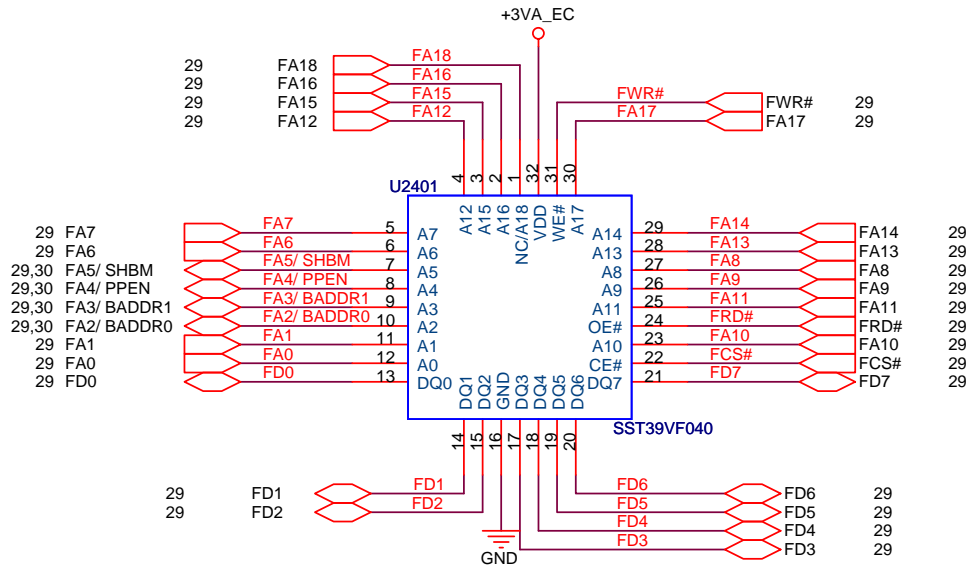
MICROPHONE IN



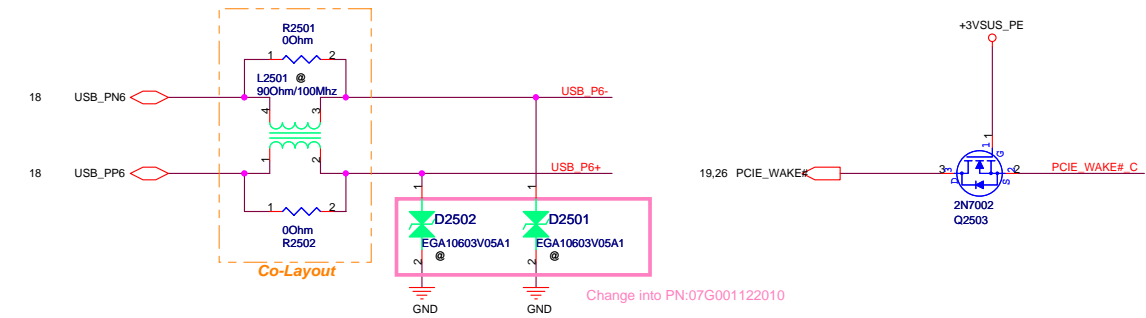
ASUS/ALPHA		Title : MIC JACK	
ASUSALPHATeK COMPUTER INC.		Engineer: Horng Chou	
Size Custom	Project Name TERESA		Rev 1.1
Date: Monday, February 05, 2007		Sheet 23 of 57	



ISA ROM



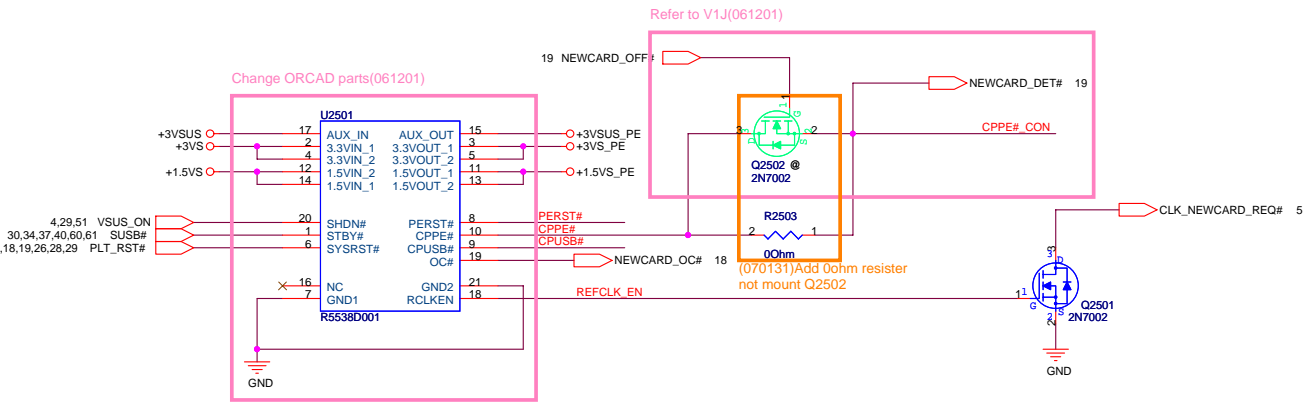
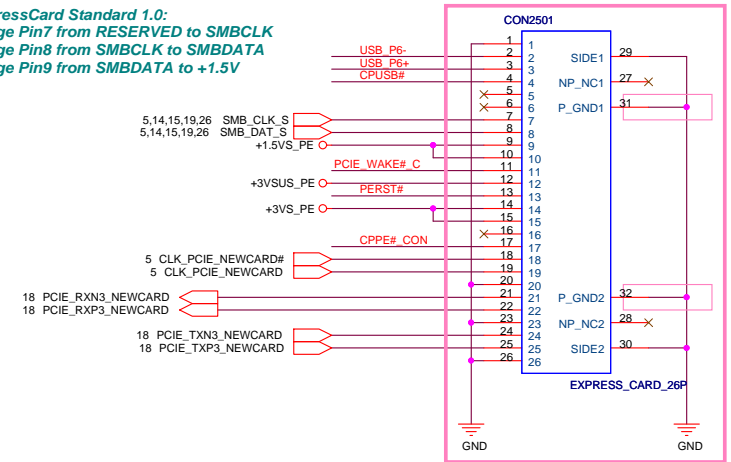
ASUSALPHA		Title : ISA ROM	
ASUSALPHATeK COMPUTER INC.		Engineer: Horng Chou	
Size	Project Name		Rev
Custom	TERESA		1.1
Date: Monday, February 05, 2007		Sheet	24 of 57



!! ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin8 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V

NewCard Header

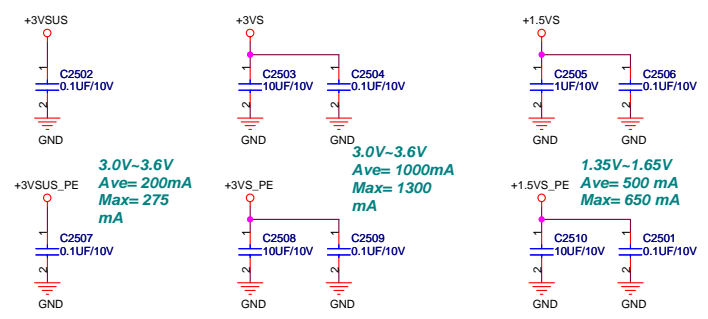
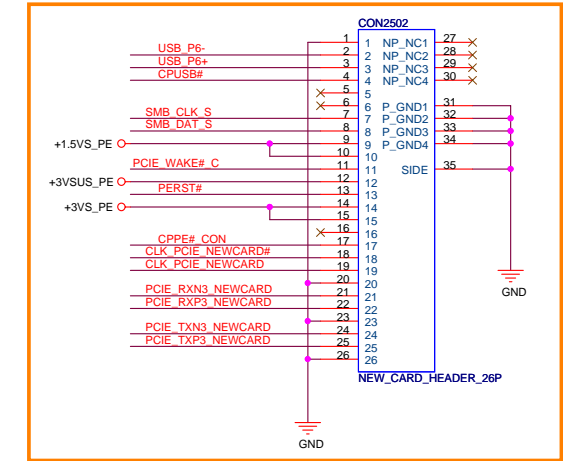
(061227)Change
 Schematic Part->EXPRESS_CARD_26P_6HOLD_SA
 PCB Footprint->nb_exp_card_26p_6hd_sa_1f2
 PN=12G161300269



(061214)NewCard Ejector was combined into Header



(070201)Add CON2502 in other to colayout with CON2501



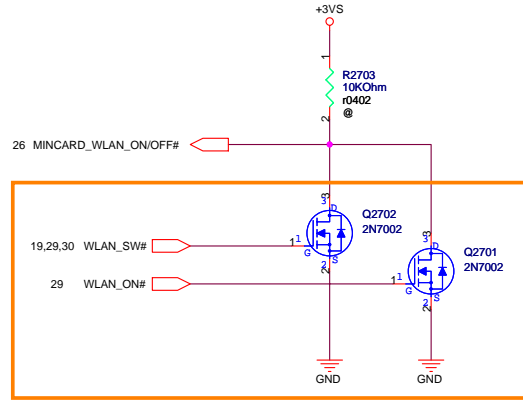
For Bluetooth

For Side SW

Delete Bluetooth CON

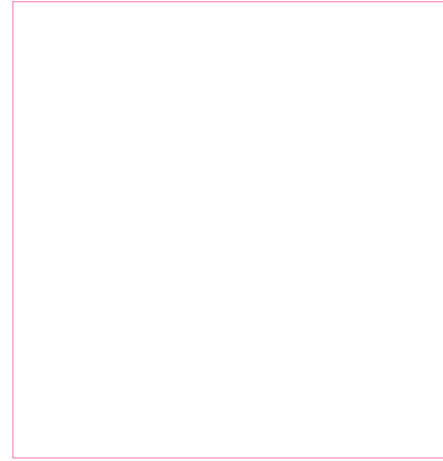


WLAN ON/OFF Control

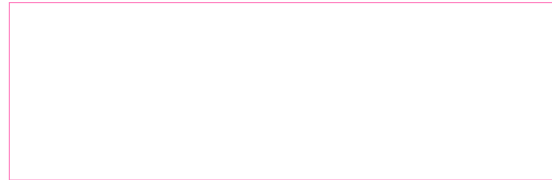


(070202)Modify WLAN on/off circuit

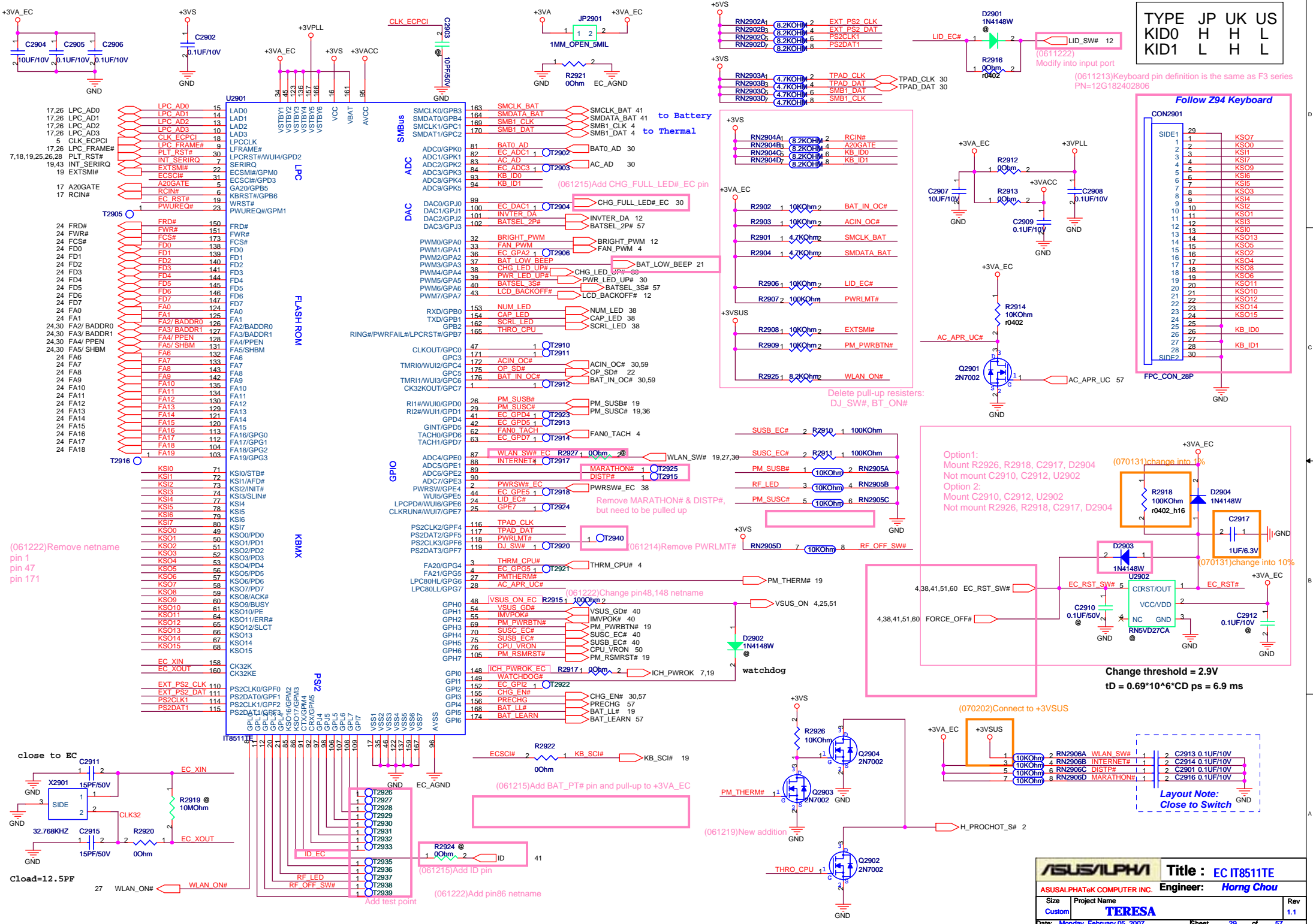
Delete BT ON/OFF Control



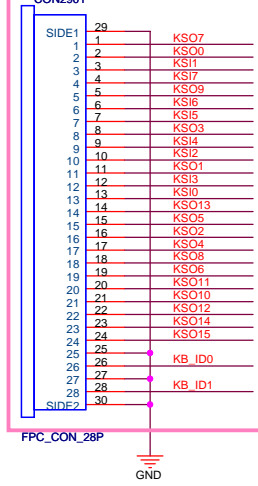
Delete FR Switch



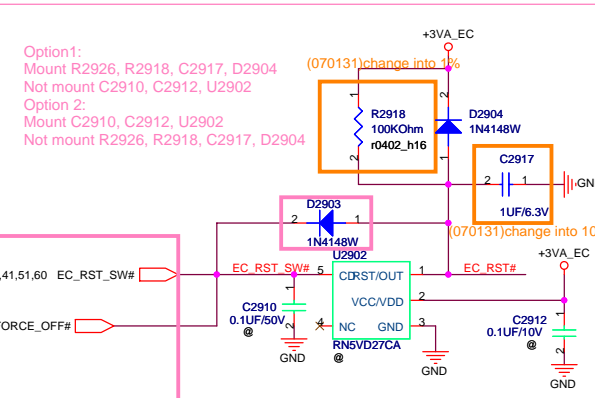
TYPE JP UK US
KID0 H H L
KID1 L H L



Follow Z94 Keyboard



FPC_CON_28P



Change threshold = 2.9V
tD = 0.69*10^6*CD ps = 6.9 ms

Option 1: Mount R2926, R2918, C2917, D2904
Not mount C2910, C2912, U2902
Option 2: Mount C2910, C2912, U2902
Not mount R2926, R2918, C2917, D2904

(070131)change into 1%
(070131)change into 10%

(070202)Connect to +3VSUS

Layout Note: Close to Switch



close to EC
Cload=12.5pF

(061222)Remove netname pin 1 pin 47 pin 171

(061215)Add CHG_FULL_LED#_EC pin

(061215)Add BAT_PT# pin and pull-up to +3VA_EC

(061219)New addition

(061215)Add ID pin

(061222)Add pin66 netname

(061215)Add ID pin

(061215)Add ID pin

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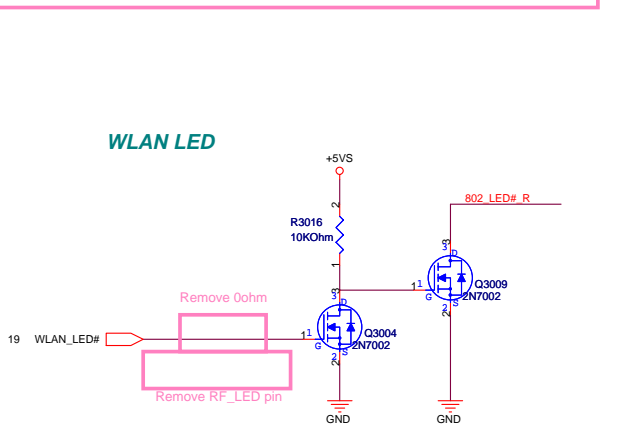
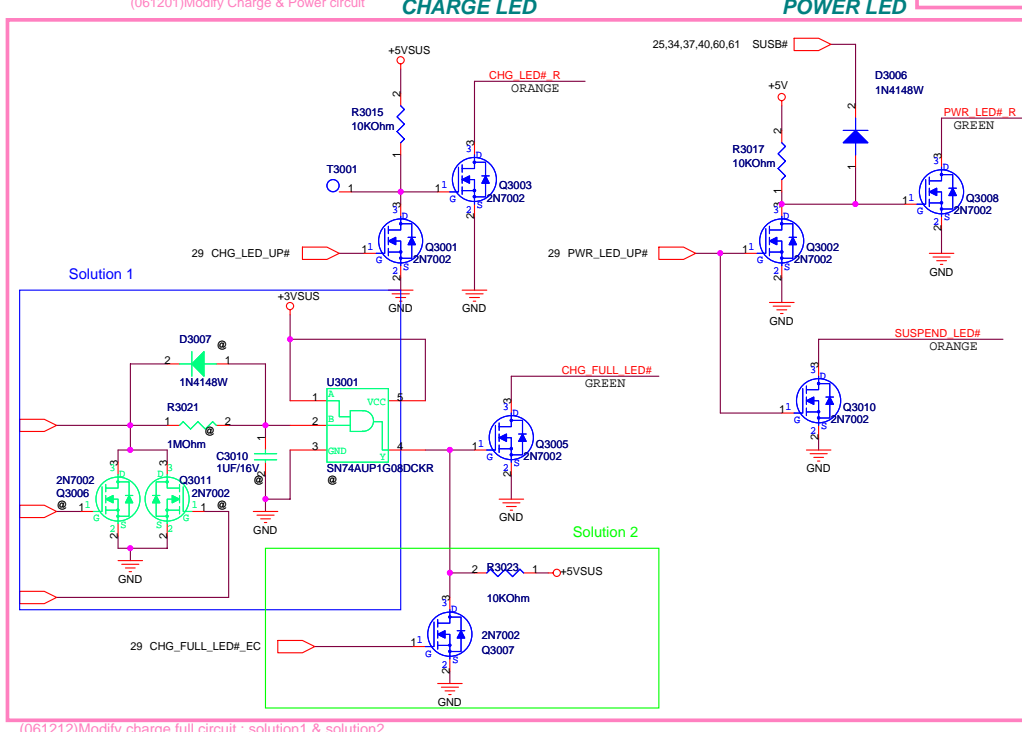
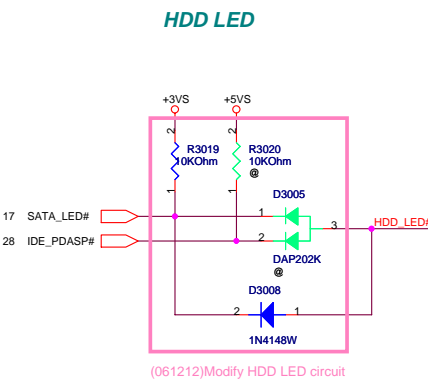
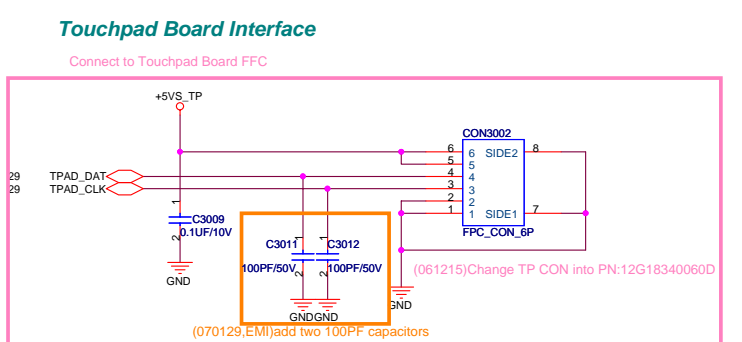
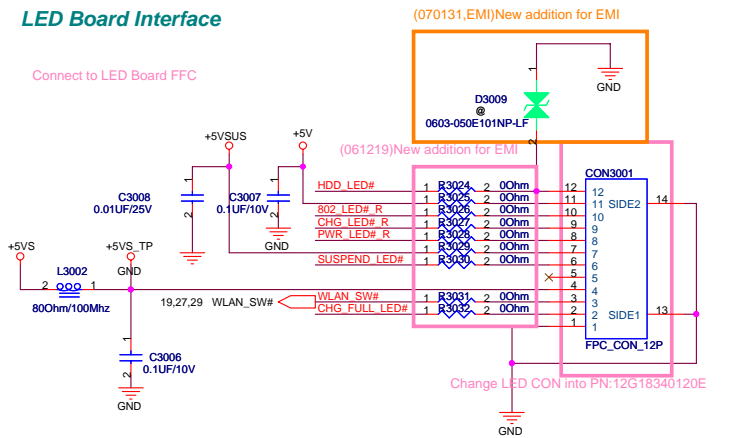
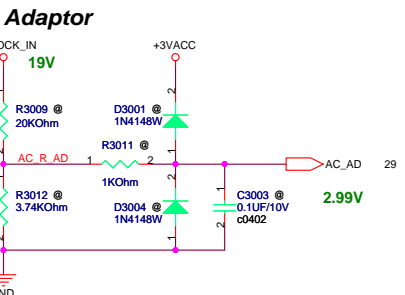
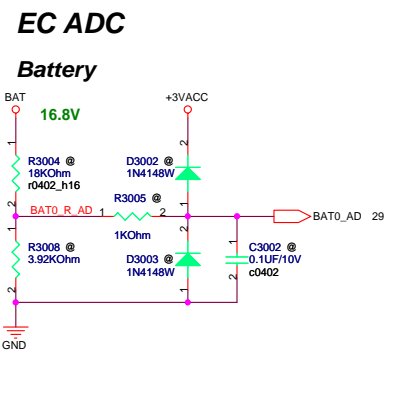
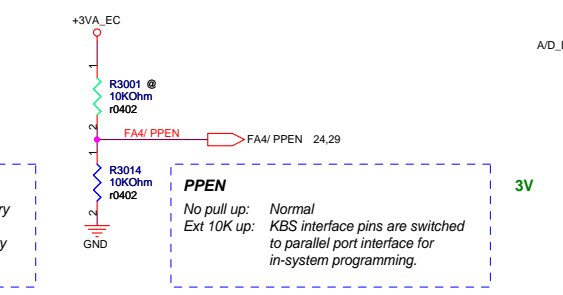
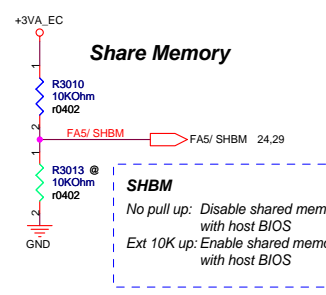
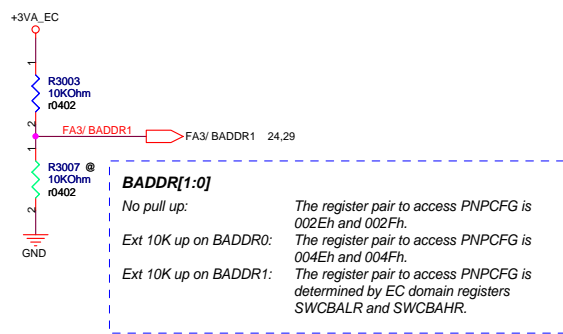
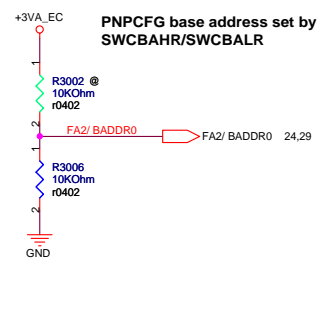
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(061215)Add ID pin

(061215)Add ID pin

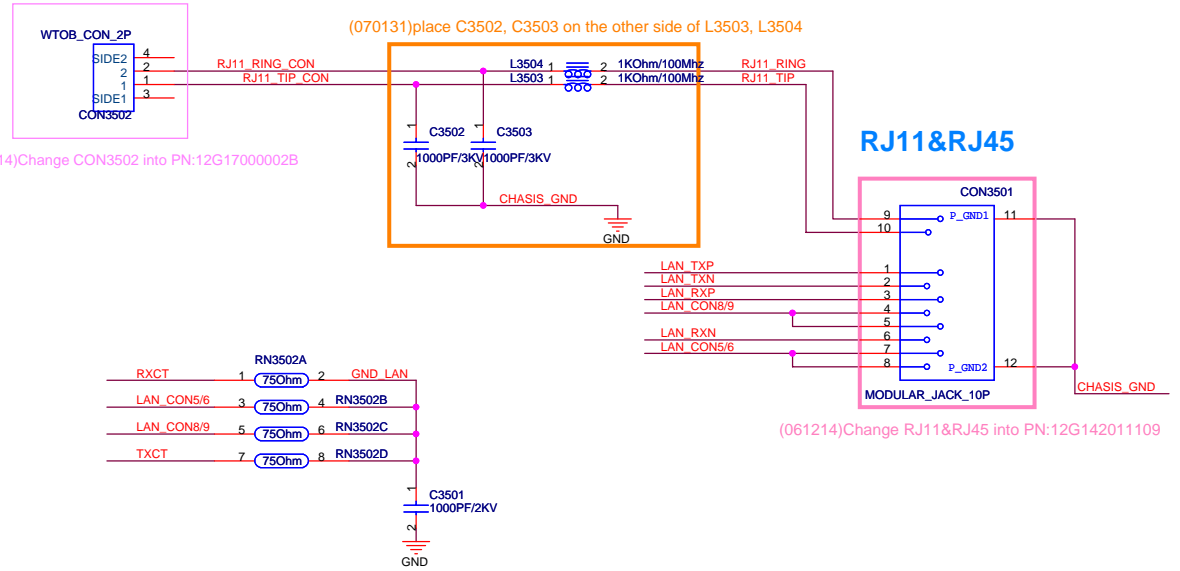
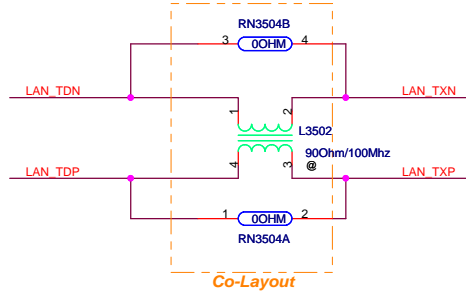
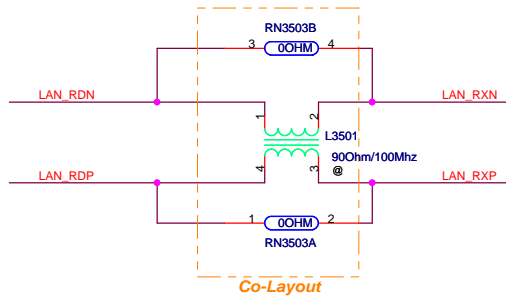
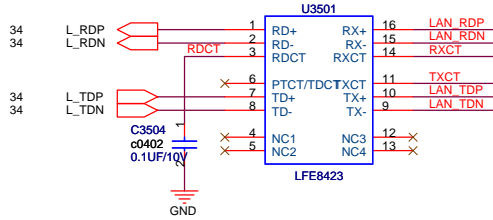
EC Hardware Strap

Strap value sampled after VSTBY power up reset



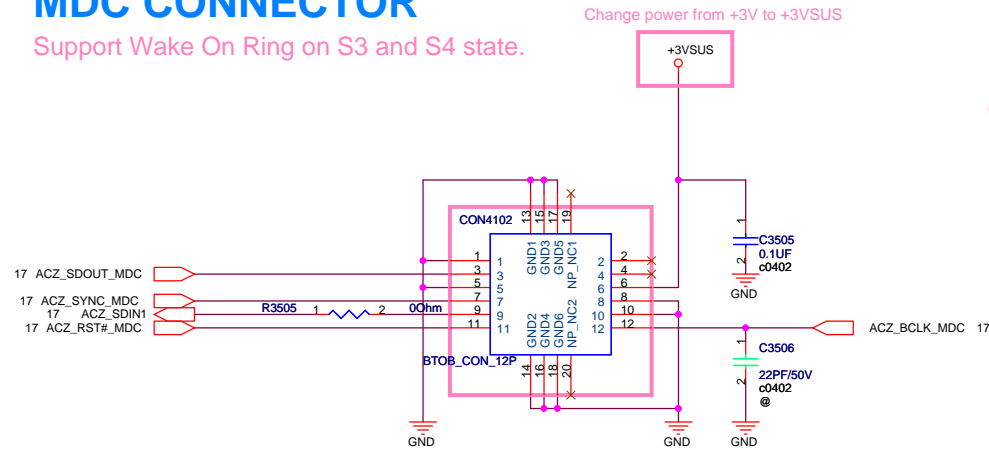
LAN PORT

TRANSFORMER 10/100MB



MDC CONNECTOR

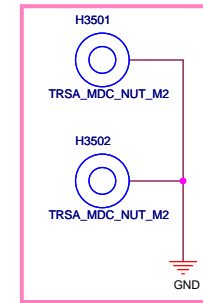
Support Wake On Ring on S3 and S4 state.



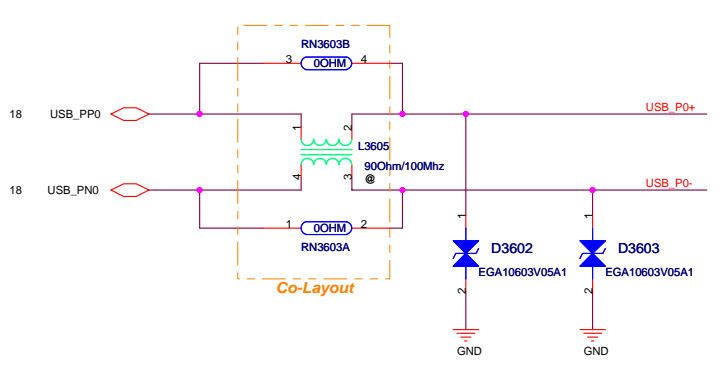
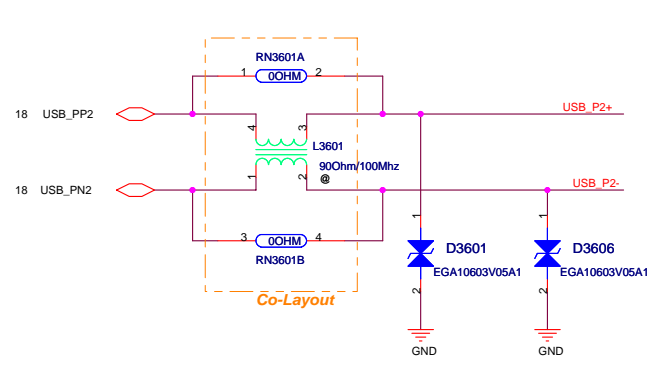
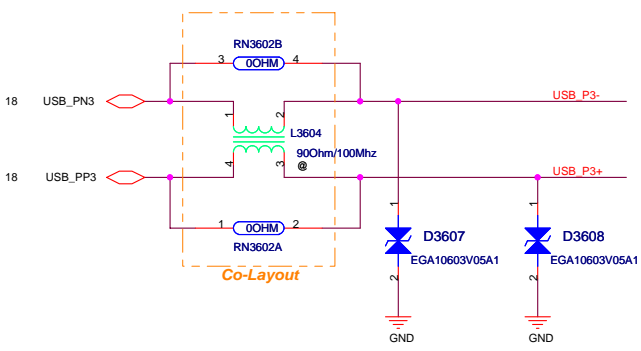
(061214)Change MDC CON into PN:12G16020012D

B:MDC NUT

(061219)Change MDC NUT into PN:13G021054000

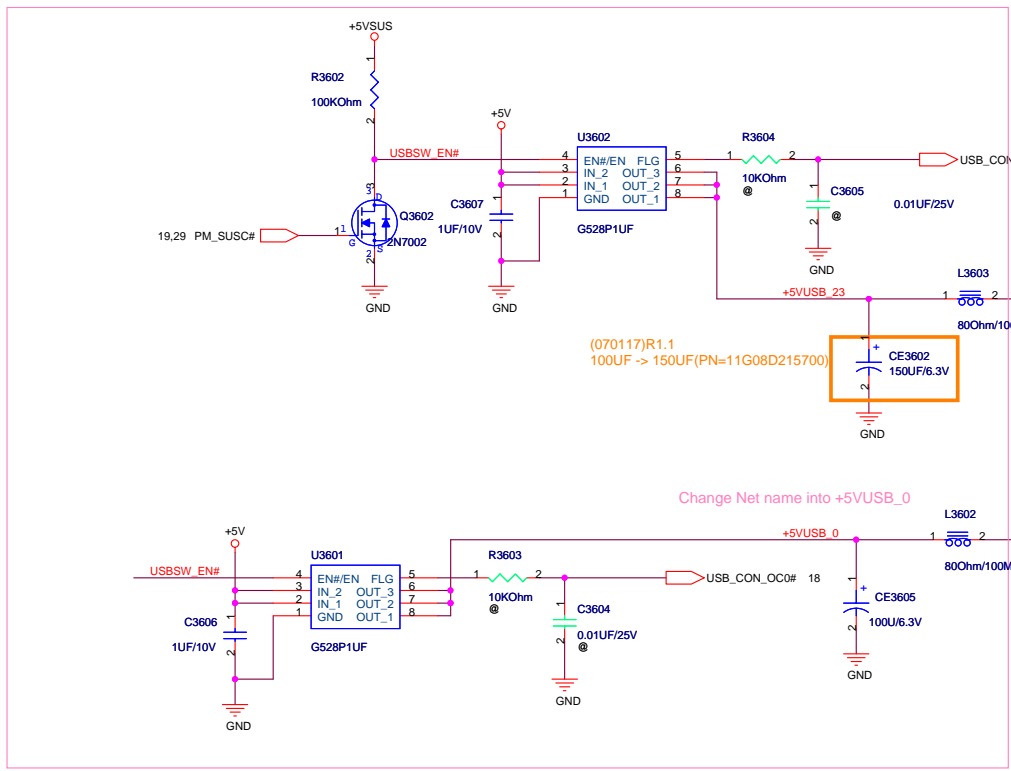


ASUS/ALPHA		Title : RJ45/RJ11/MDC	
ASUSALPHATEK COMPUTER INC.		Engineer: Horng Chou	
Size	Project Name	Rev	
Custom	TERESA	1.1	
Date: Monday, February 05, 2007		Sheet 35 of 57	

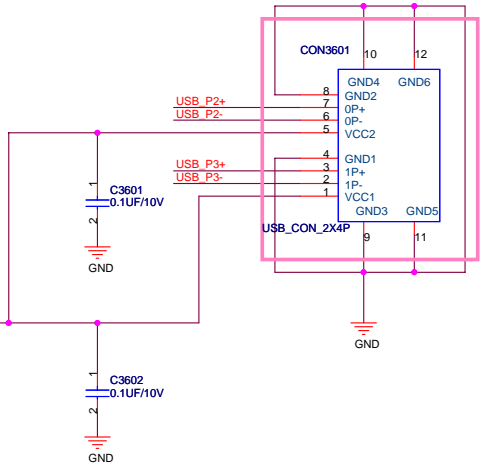


Delete N-MOSFET PMN45EN

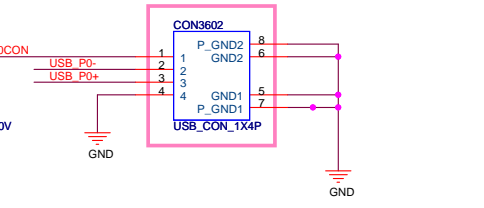
Add USB Switch

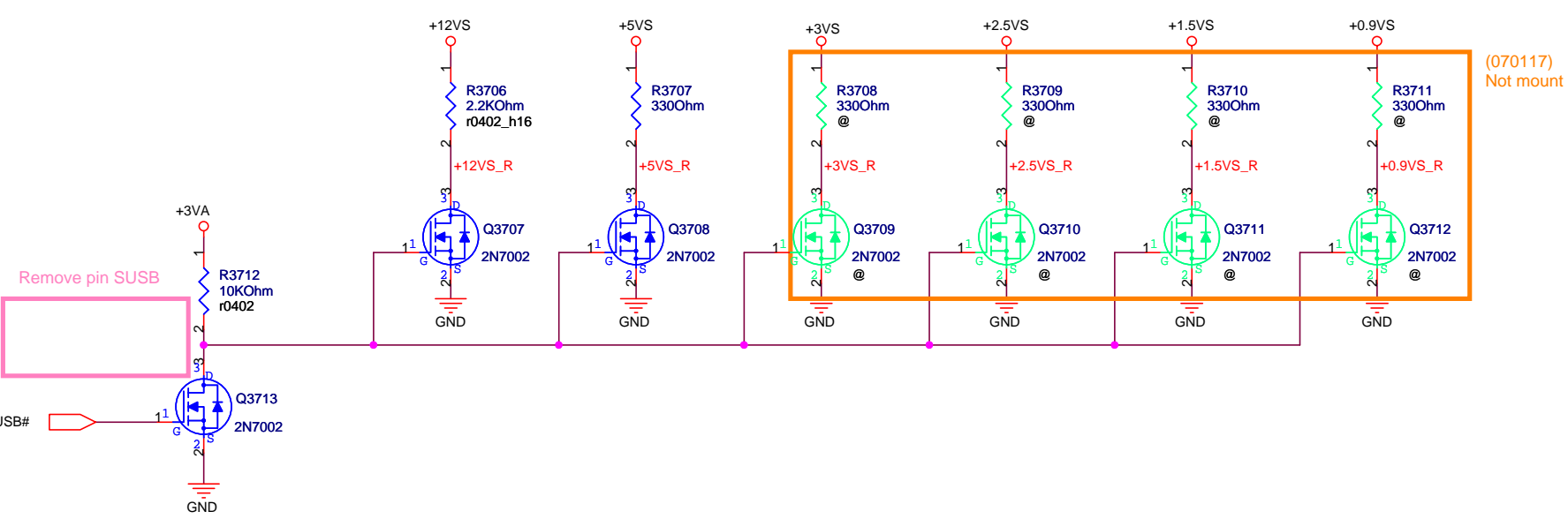
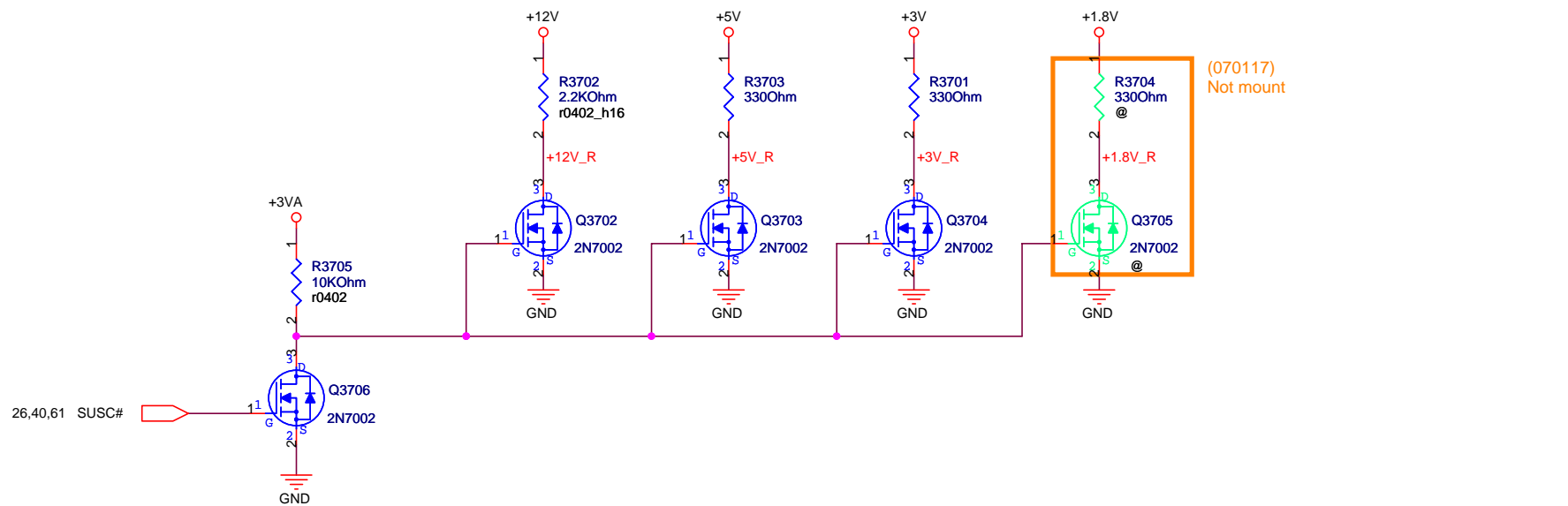


(06121)Change USB CON into PN:12G13111108F



(061206)Change USB CON into PN:12G131030043

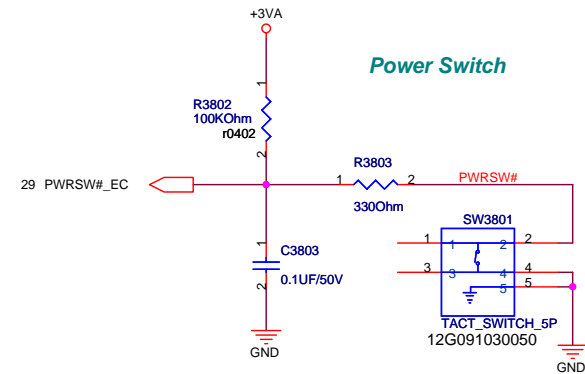




ASUS/ALPHA		Title : Discharge Circuit	
ASUSALPHATEK COMPUTER INC.		Engineer: Hong Chou	
Size Custom	Project Name TERESA	Rev 1.1	
Date: Monday, February 05, 2007		Sheet 37 of 57	

Main Board SW & LED

Power LED move to daughter board



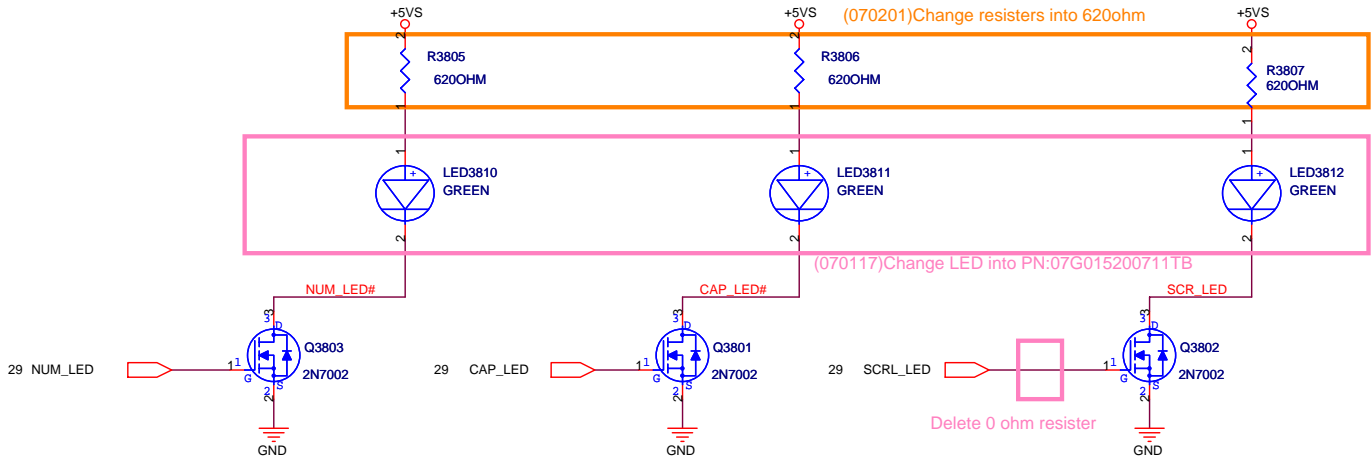
Delete RF LED and Power4 Gear LED

Delete RF/Touchpad and Power4 Gear SWITCH

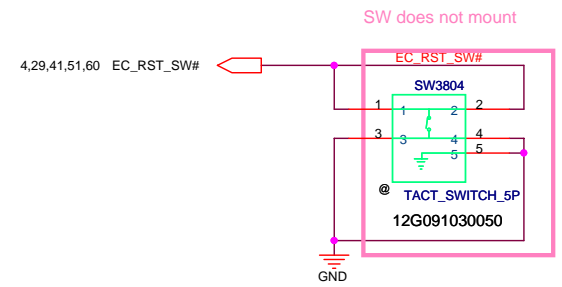
NUMBER LOCK LED

CAPS LOCK LED

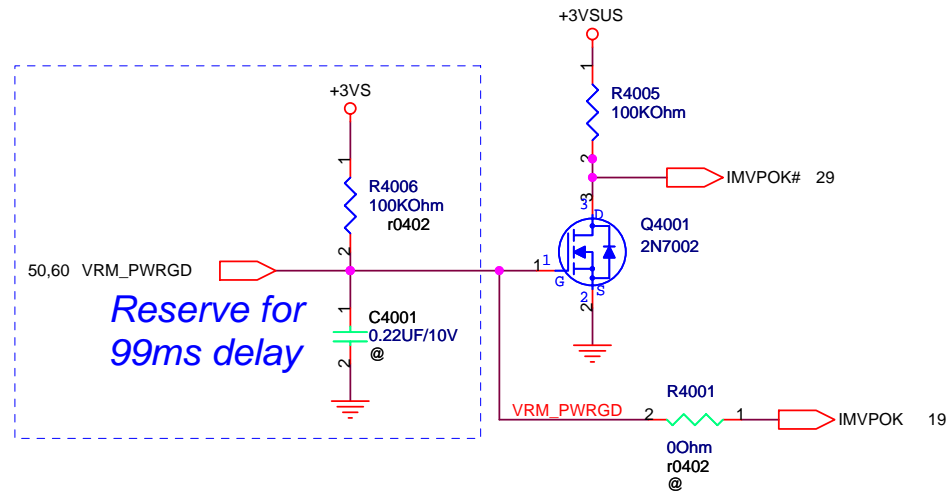
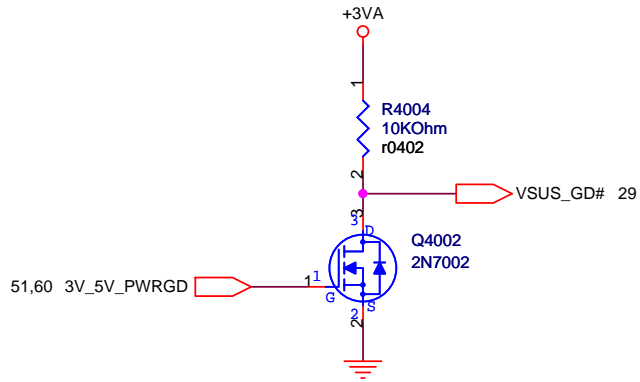
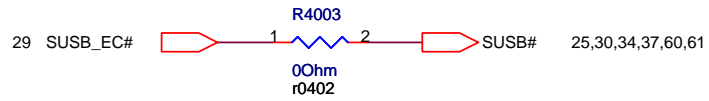
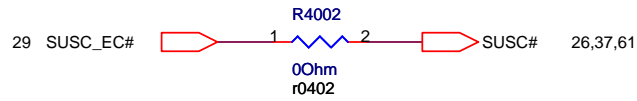
SCROLL LOCK LED



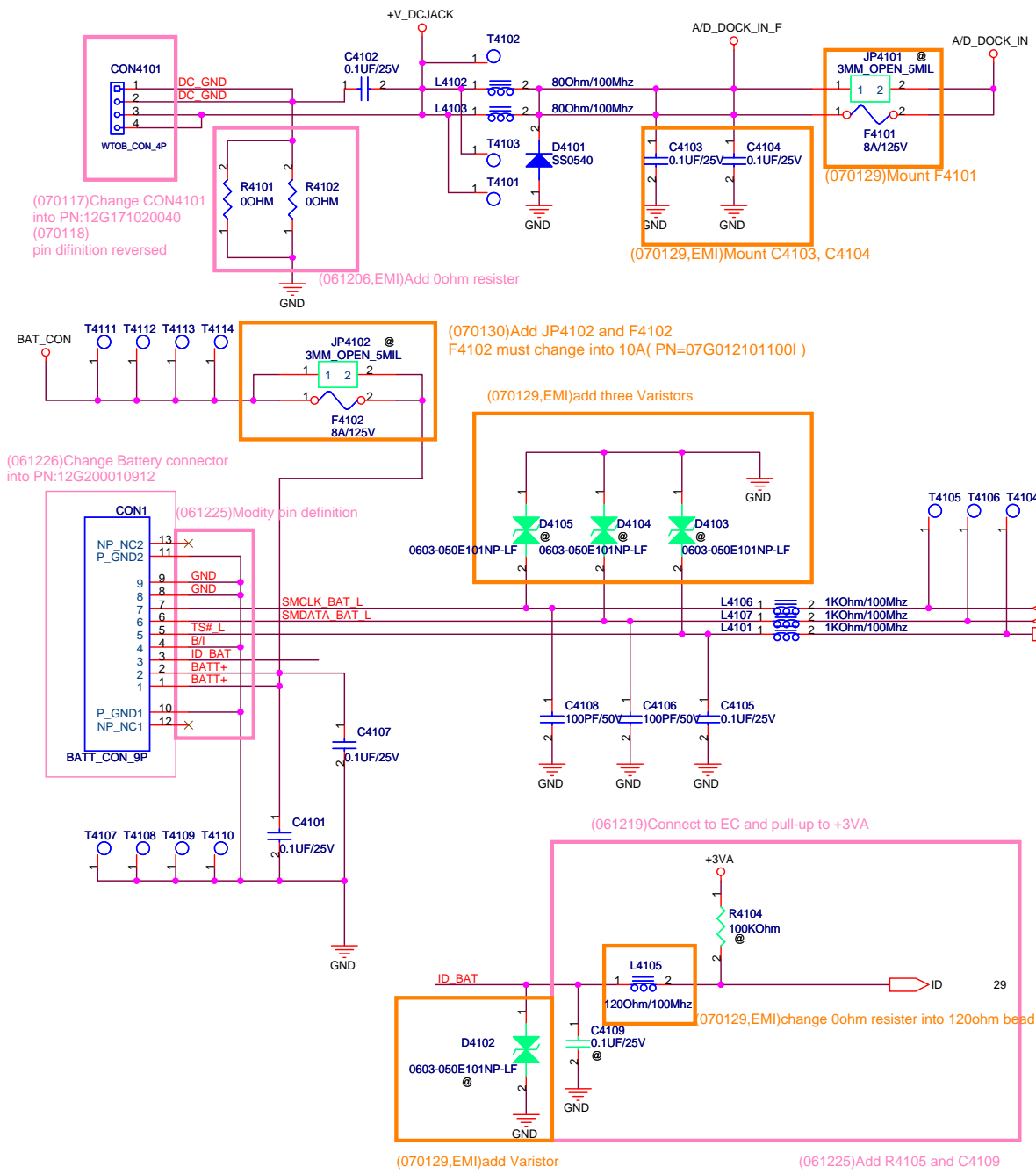
Reset Switch



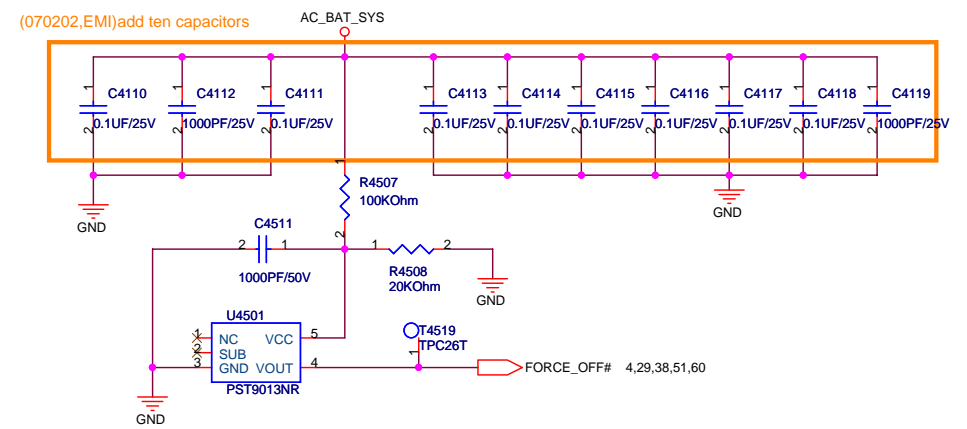
ASUS/ALPHA		Title : SW/LED	
ASUSALPHATeK COMPUTER INC.		Engineer: Horng Chou	
Size Custom	Project Name TERESA	Rev 1.1	
Date: Monday, February 05, 2007		Sheet 38 of 57	



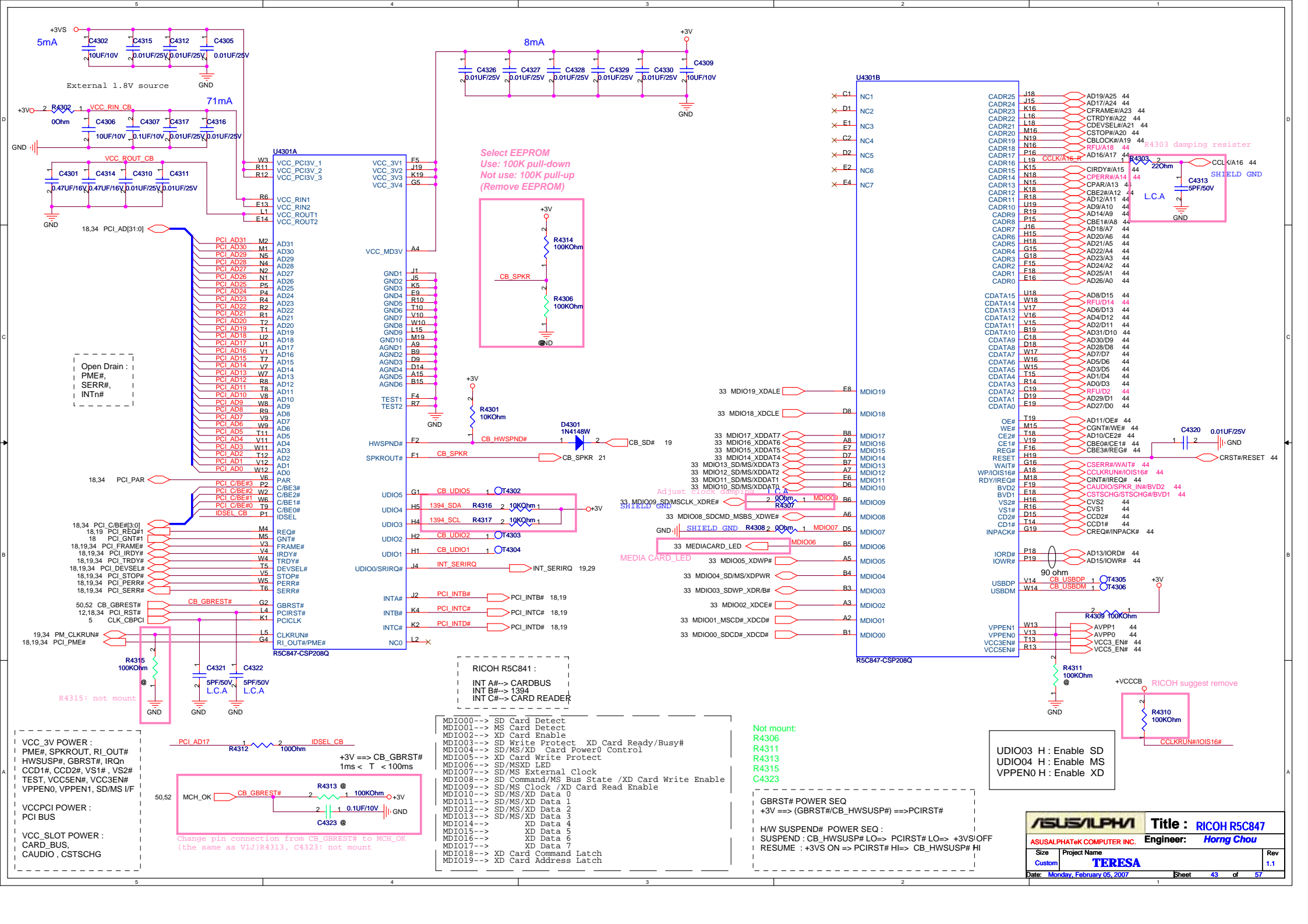
DC Power Jack



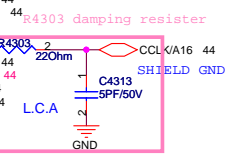
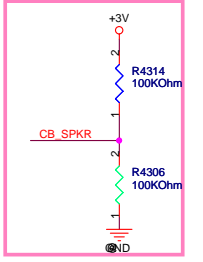
Without Battery & Pull out Adapter



ASUSALPHA		Title : DC/ BATT IN	
ASUSALPHATeK COMPUTER INC.		Engineer: Horng Chou	
Size Custom	Project Name TERESA	Rev 1.1	
Date: Monday, February 05, 2007		Sheet 41 of 57	



Select EEPROM
Use: 100K pull-down
Not use: 100K pull-up
(Remove EEPROM)



RICOH R5C841 :
INT A#-> CARDBUS
INT B#-> 1394
INT C#-> CARD READER

MDIO00-->	SD Card Detect
MDIO01-->	MS Card Detect
MDIO02-->	XD Card Enable
MDIO03-->	SD Write Protect / XD Card Ready/Busy#
MDIO04-->	SD/MS/XD Card Power0 Control
MDIO05-->	XD Card Write Protect
MDIO06-->	SD/MSXD LED
MDIO07-->	SD/MS External Clock
MDIO08-->	SD Command/MS Bus State /XD Card Write Enable
MDIO09-->	SD/MS Clock /XD Card Read Enable
MDIO10-->	SD/MS/XD Data 0
MDIO11-->	SD/MS/XD Data 1
MDIO12-->	SD/MS/XD Data 2
MDIO13-->	SD/MS/XD Data 3
MDIO14-->	XD Data 4
MDIO15-->	XD Data 5
MDIO16-->	XD Data 6
MDIO17-->	XD Data 7
MDIO18-->	XD Card Command Latch
MDIO19-->	XD Card Address Latch

Not mount:
R4306
R4311
R4313
R4315
C4323

GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==> PCIRST#

HW SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3V/OFF
RESUME : +3V ON => PCIRST# HI=> CB_HWSUSP# HI

UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD

ASUS/ALPHA Title : **RICOH R5C847**
ASUSALPHATeK COMPUTER INC. Engineer: **Horng Chou**

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Monday, February 05, 2007 Sheet 43 of 57

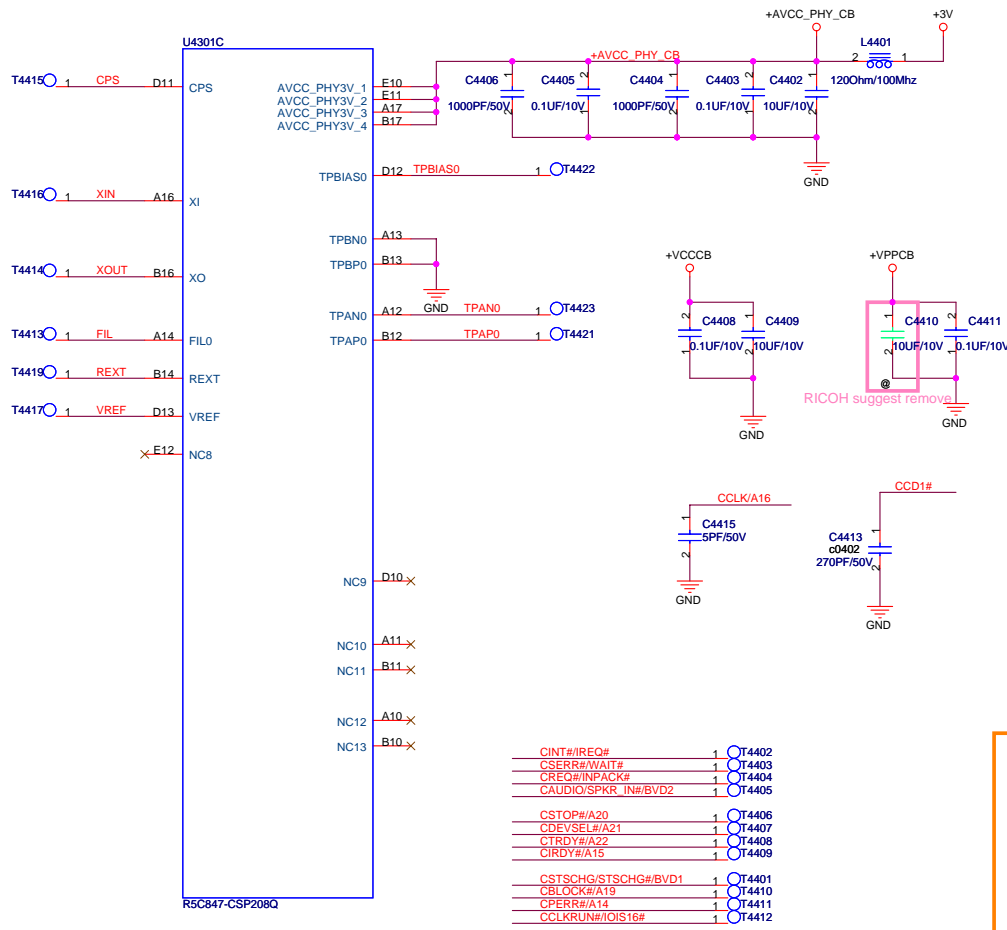
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1#, VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F

VCCPCI POWER :
PCI BUS

VCC_SLOT POWER :
CARD_BUS,
AUDIO, CSTSCHG

Change pin connection from CB_GBRST# to MCH_OK
(the same as V1) R4313, C4323: not mount

PCMCIA SOCKET

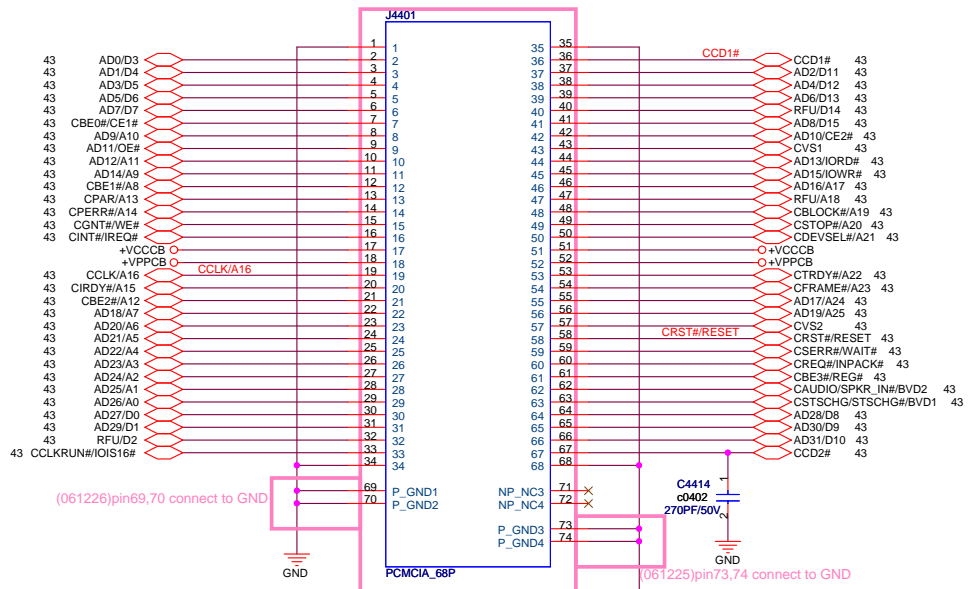


- CINT#/IREQ# 1 T4402
- CSERR#/WAIT# 1 T4403
- CREG#/INPACK# 1 T4404
- CAUDIO/SPKR_IN#/BVD2 1 T4405
- CSTOP#/A20 1 T4406
- CDEVSEL#/A21 1 T4407
- CTRDY#/A22 1 T4408
- CIRDY#/A15 1 T4409
- CSTSCHG#/STSCHG#/BVD1 1 T4401
- CBLOCK#/A19 1 T4410
- CPERR#/A14 1 T4411
- CCLKRUN#/IOIS16# 1 T4412

CCD1# CCD2# 16bit
L OTHER 32bit

Not mount:
C4410

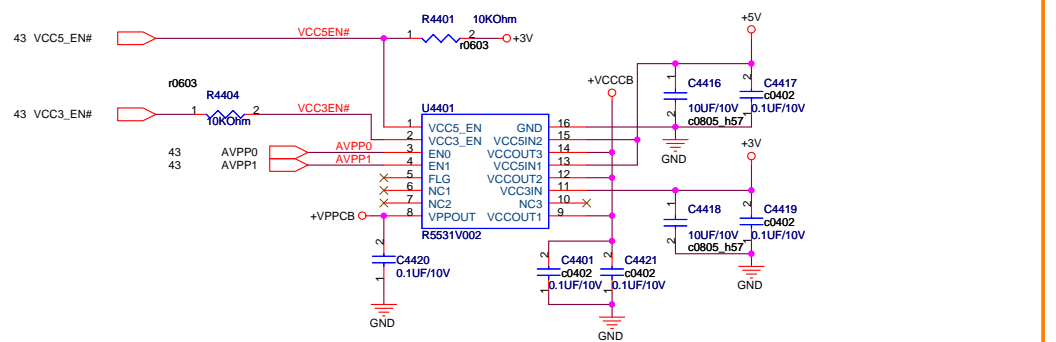
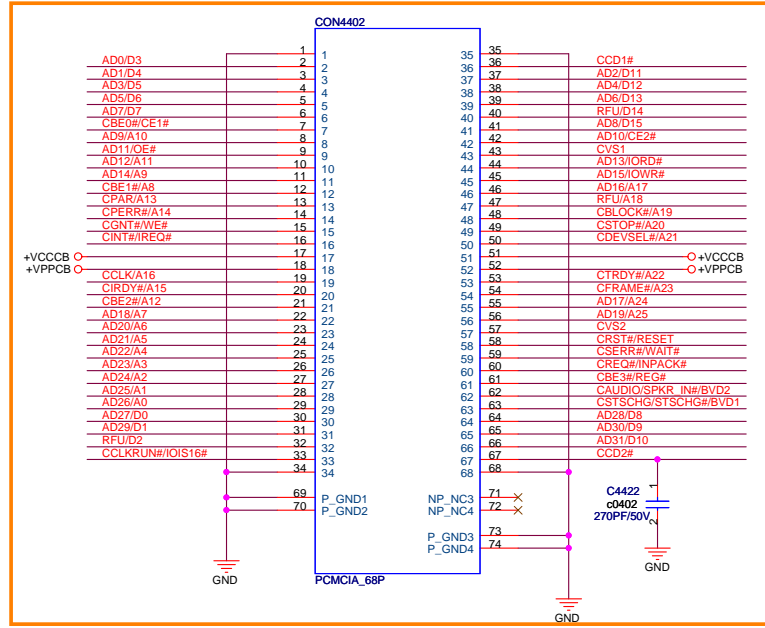
(061227)Change PCB footprint
PN=12G16040068Y



(061226)pin69,70 connect to GND

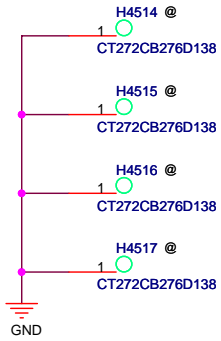
(061225)pin73,74 connect to GND

(070131)Add PCMCIA Socket



A:CPU BKT

PN:s01756



B:MDC NUT

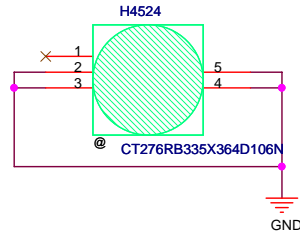
MDC NUT put on page35 (H3501, H3502)

F:MINI CARD NUT

MINI CARD NUT put on page26(H2601, H2602)

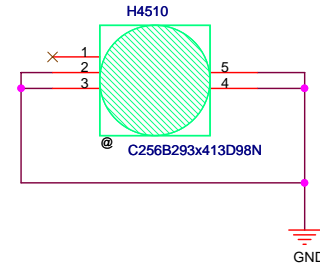
C:TOP TO BTM

PN:S01912



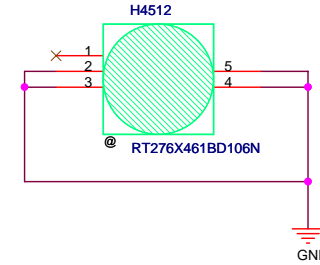
D:FIX MB

PN:s01769



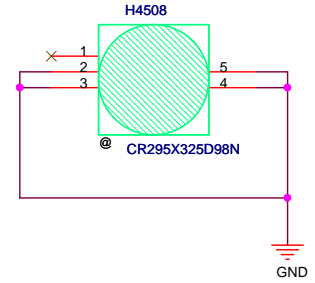
E:TOP TO BTM

PN:S01911



G:FIX MB

PN:s01783



H:SYS BOSS

PN:S01914

I:MB TO IO BKT

PN:S01913

J:SYS BOSS

PN:S01915

K:MB TO IO BKT

PN:S01705

L:TOP TO BTM

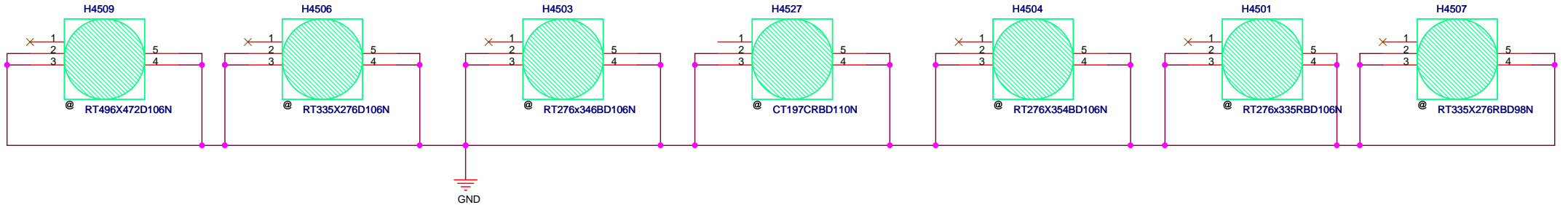
PN:S01916

M:SYS BOSS

PN:s01917

N:TOP TO BTM

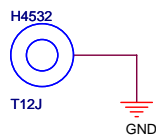
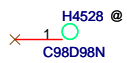
PN:S01851



O:ALIGNMENT HOLE T:NB SINK NUT

PN:temp_5262_gh15

PN:13GNJ510M170-1

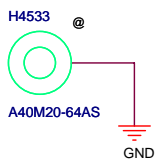


P:ALIGNMENT HOLE

PN:s01724



EMI NUT for LVDS cable
PN:13G021029050



U:TOP TO BTM

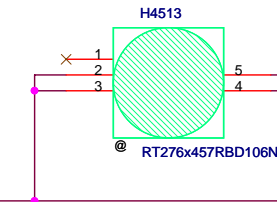
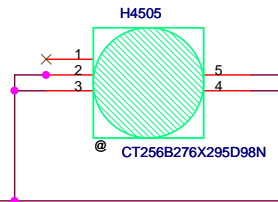
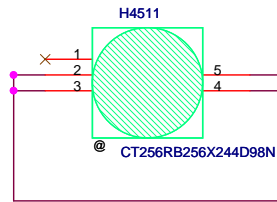
PN:S01854

V:TOP TO BTM

PN:S01857

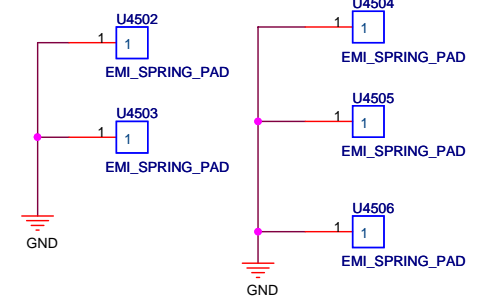
W:TOP TO BTM

PN:S01918

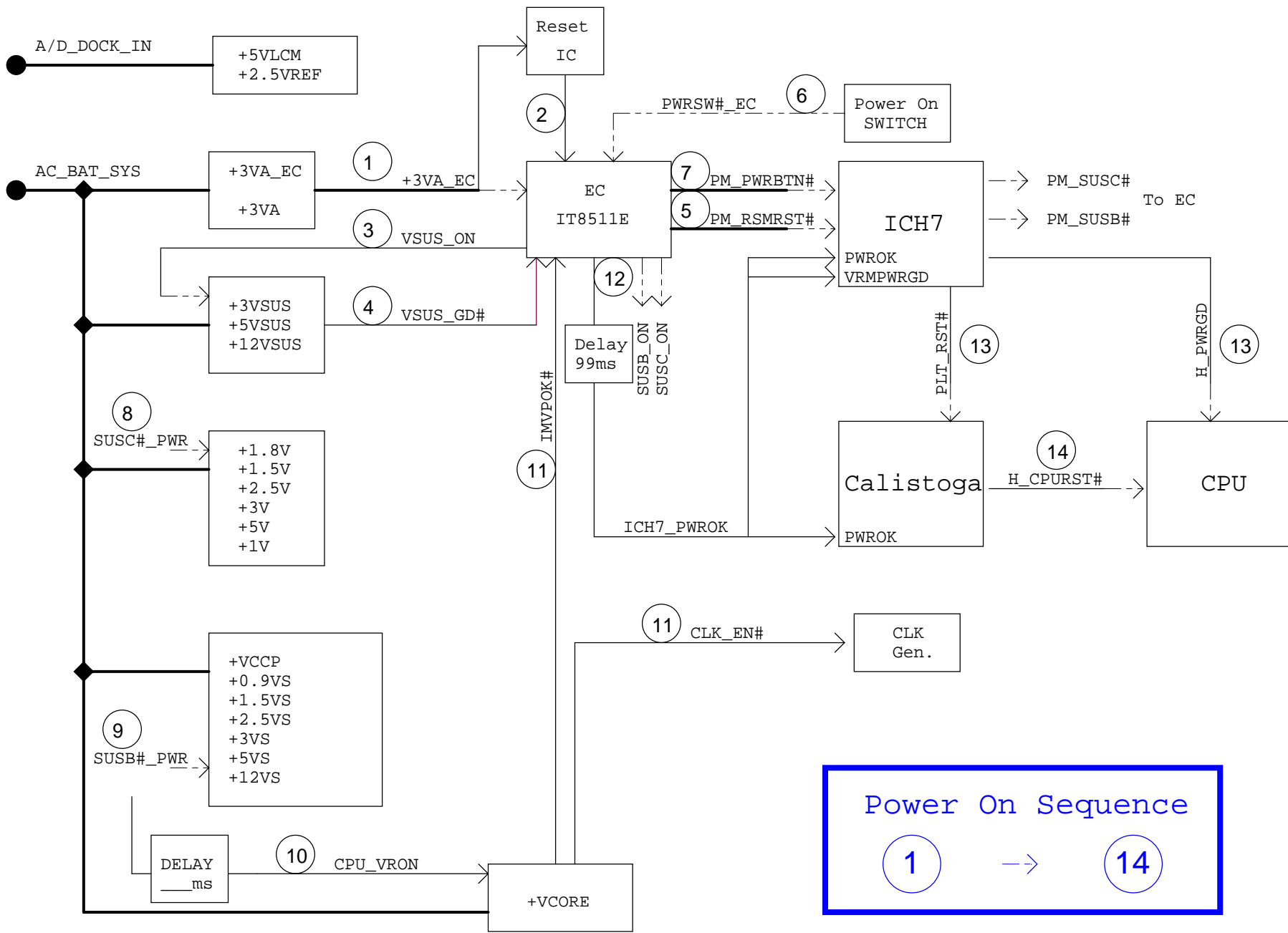


EMI SPRING

PN:13G021034050



ASUS/ALPHA		Title : SCREW HOLE	
ASUSALPHATeK COMPUTER INC.		Engineer: Hong Chou	
Size Custom	Project Name TERESA	Rev 1.1	
Date: Monday, February 05, 2007	Sheet	45	of 57



Power On Sequence

① → ⑭

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM	O	48	GPH0	VSUS_ON_EC	O
33	PWM1/GPA1	FAN_PWM	O	54	GPH1	VSUS_GD#	I
36	PWM2/GPA2	/	O	55	GPH2	IMVPOK#	I
37	PWM3/GPA3	BAT_LOW_BEEP(Reserved)	O	69	GPH3	PM_PWRBTN#	O
38	PWM4/GPA4	CHG_LED_UP#	O	70	GPH4	SUSC_EC#	O
39	PWM5/GPA5	PWR_LED_UP#	O	75	GPH5	SUSB_EC#	O
40	PWM6/GPA6	BATSEL_3S#	O	76	GPH6	CPU_VRON	O
43	PWM7/GPA7	LCD_BACKOFF#	O	105	GPH7	PM_RSMRST#	O
153	RXD/GPB0	NUM_LED	O	148	GPIO	ICH_PWROK_EC	O
154	TXD/GPB1	CAP_LED	O	149	GPIO1	WATCHDOG#	O
162	GPB2	SCRL_LED	O	152	GPIO2	/	
163	SMCLK0/GPB3	SMCLK_BAT	I/O	155	GPIO3	CHG_EN#	O
164	SMDAT0/GPB4	SMDATA_BAT	I/O	156	GPIO4	PRECHG	O
5	GA20/GPB5	A20GATE	O	168	GPIO5	BAT_LL#	O
6	KBRST#/GPB6	RCIN#	O	174	GPIO6	BAT_LEARN	O
165	GPB7	THRO_CPU	O	109	GPIO7	/	
47	CLKOUT/GPC0	/	O	99	DAC0/GPJ0	CHG_FULL_LED#_EC	O
169	SMCLK1/GPC1	SMB1_CLK	I/O	100	DAC1/GPJ1	/	
170	SMDAT1/GPC2	SMB1_DAT	I/O	101	DAC2/GPJ2	INVTDR_DA	O
171	GPC3	/	I	102	DAC3/GPJ3	BATSEL_2P#	O
172	TMR10/WUI2/GPC4	ACIN_OC#	I	97	GPJ4	/	
175	GPC5	OP_SD#	O	98	GPJ5	/	
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I	/	/	/	
1	CK32KOUT/GPC7	/	O	/	/	/	
26	RI1#WUI0/GPD0	PM_SUSB#	I	81	ADC0/GPK0	BAT0_AD	I
29	RI2#WUI1/GPD1	PM_SUSC#	I	82	ADC1/GPK1	/	
30	LPCRST#WUI4//GPD2	PLT_RST#	I	83	ADC2/GPK2	AC_AD	I
31	ECSC#GPD3	ECSC#	O	84	ADC3/GPK3	/	
41	GPD4	/		93	ADC8/GPK4	KB_ID0	I
42	GINT/GPD5	/		94	ADC9/GPK5	KB_ID0	I
62	TACH0/GPD6	FANO_TACH	I	/	/	/	
63	TACH1/GPD7	/	O	/	/	/	
87	ADC4/GPE0	WLAN_SW#_EC(Reserved)	I	8	GPL0	/	O
88	ADC5/GPE1	/	I	11	GPL1	/	O
89	ADC6/GPE2	/	I	12	GPL2	/	I
90	ADC7/GPE3	/	I	20	GPL3	/	O
2	PWRSW/GPE4	PWRSW#_EC	I	21	GPL4	/	
44	WUI5/GPE5	/		106	GPL5	/	
24	LPCPD#WUI6/GPE6	LID_EC#	I	107	GPL6	/	
25	CLKRUN#WUI7/GPE7	/	O	108	GPL7	/	
110	PS2CLK0/GPF0	/		22	ECSMH#GPM0	EXTSM#	O
111	PS2DAT0/GPF1	/		23	PWUREQ#GPM1	/	
114	PS2CLK1/GPF2	/	I/O	85	KSO16/GPM2	/	
115	PS2DAT1/GPF3	/	I/O	86	KSO17/GPM3	ID_EC (Reserved)	I
116	PS2CLK2/GPF4	TPAD_CLK		91	CTX/GPM4	/	
117	PS2DAT2/GPF5	TPAD_DAT		92	CRX/GPM5	/	
118	PS2CLK3/GPF6	/		/	/	/	
119	PS2DAT3/GPF7	/	I	/	/	/	
113	FA16/GPG0	FA16					
112	FA17/GPG1	FA17					
104	FA18/GPG2	FA18					
103	FA19/GPG3	/					
3	FA20/GPG4	THRM_CPU#	I				
4	FA21/GPG5	/					
27	LPC80HL/GPG6	PMTHERM#	O				
28	LPC80LL/GPG7	AC_APR_UC#	I				

ICH7-M GPIO SETTING

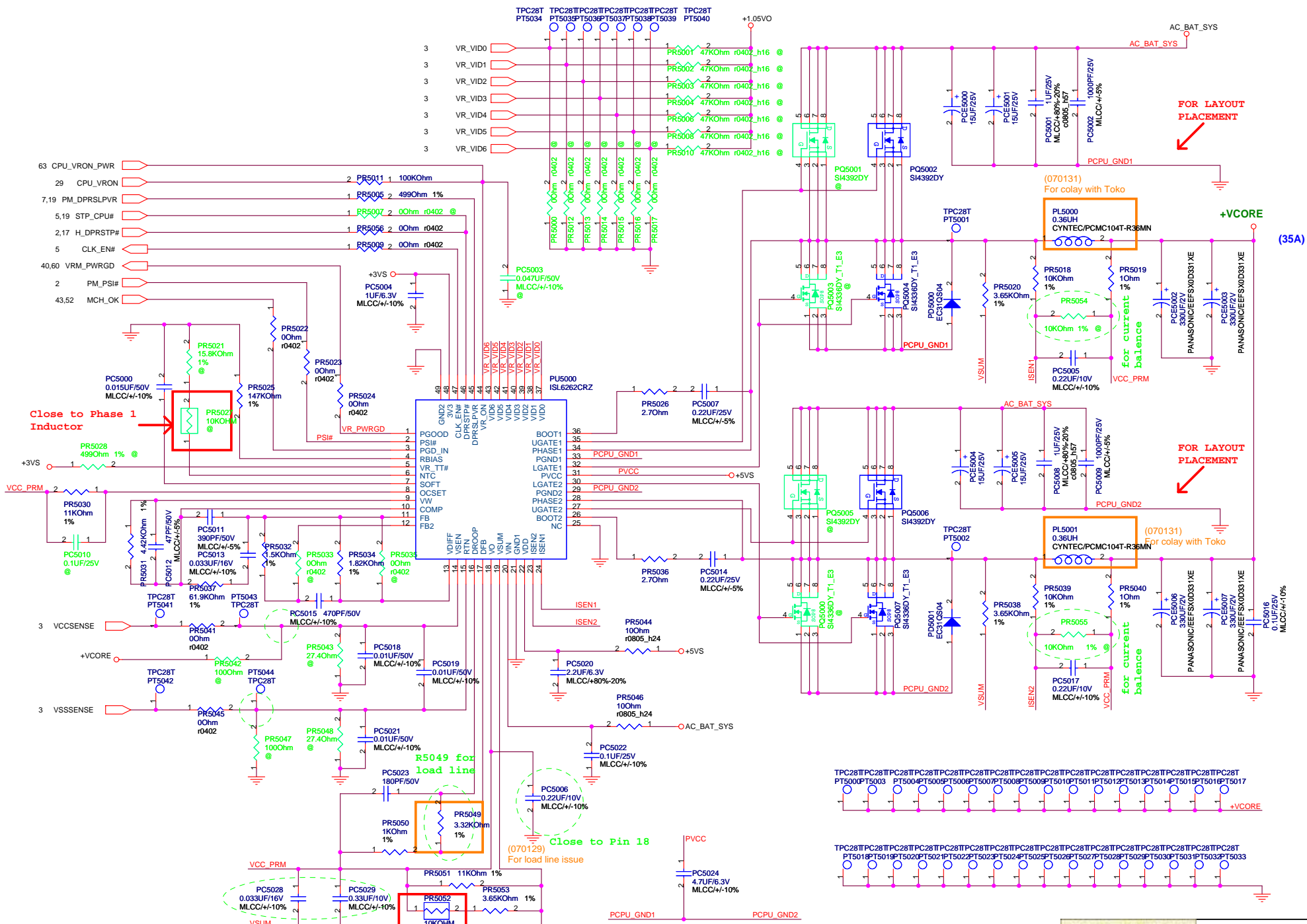
Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INT#	I
AC21	GPIO06	/	I/O
AC18	GPIO07	PM_THERM#_GPIO (Reserved)	I
E21	GPIO08	EXTSM#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	WLAN_SW#_ICH	I
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SC#	I
E19	GPIO13	NEWCARD_DET#	I
R4	GPIO14	BAT_LL#_ICH (Reserved)	I
E22	GPIO15	WLAN_LED#	O
AC22	GPIO16	PM_DPRSPLVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STPPC#	STP_PC#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STPCPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	REQ4#/GPIO22	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	/	
R3	GPIO24	/	
D20	GPIO25	CB_SD#	O
A21	GPIO26	/	
B21	GPIO27	BTO_DEV0	I
E23	GPIO28	NEWCARD_OFF#	O
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	I/O
AC19	GPIO33/AZ_DOCK_EN#	BTO_DEV1	I
U2	GPIO34/AZ_DOCK_RST#	BTO_DEV2	I
AD21	GPIO35	/	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

Indigo: the same as T12F
Pink: different from T12F

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIe Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)



FOR LAYOUT PLACEMENT

FOR LAYOUT PLACEMENT

Close to Phase 1 Inductor

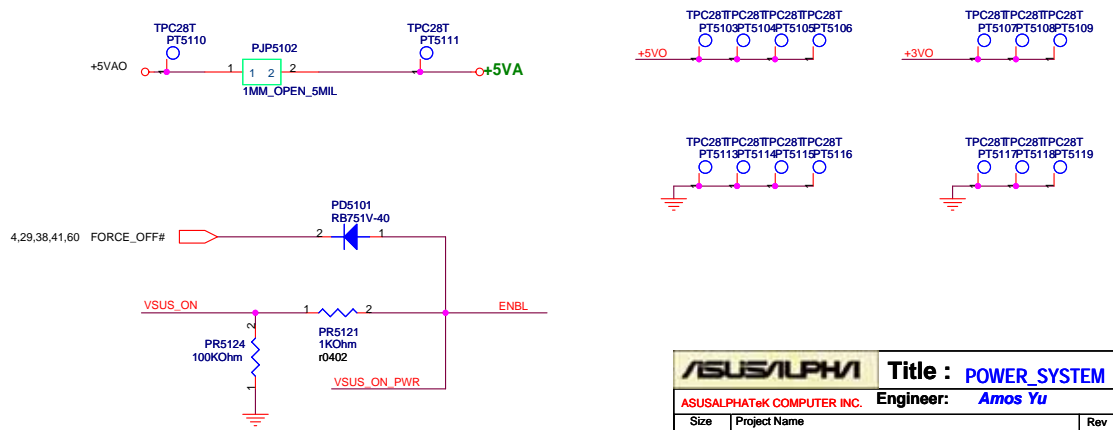
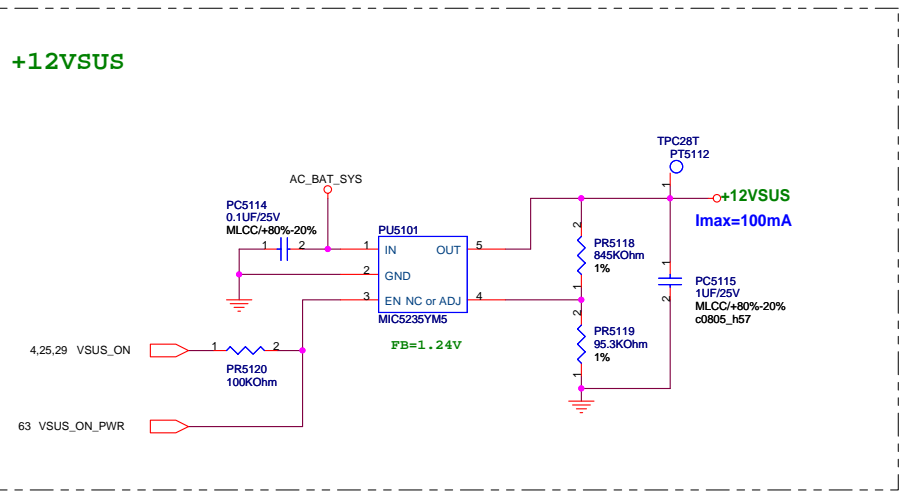
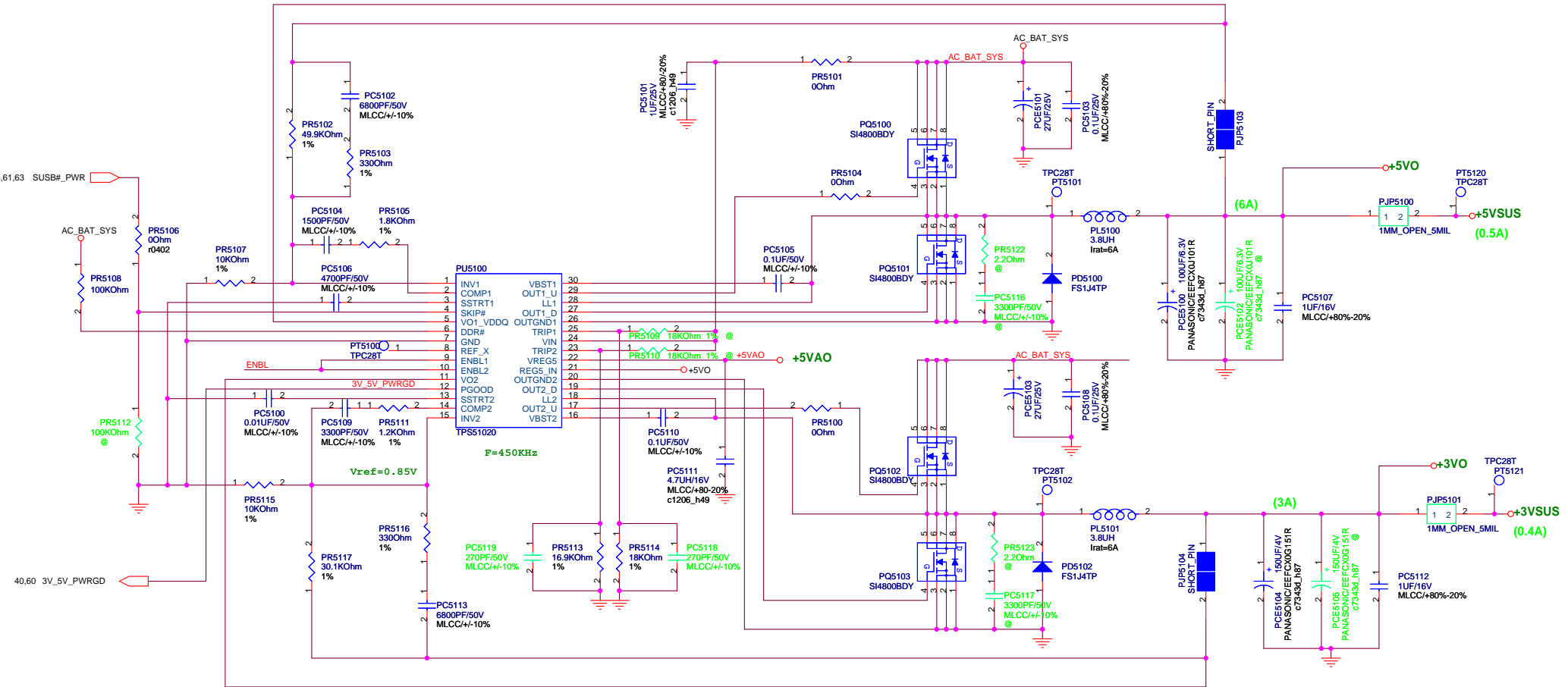
R5049 for load line

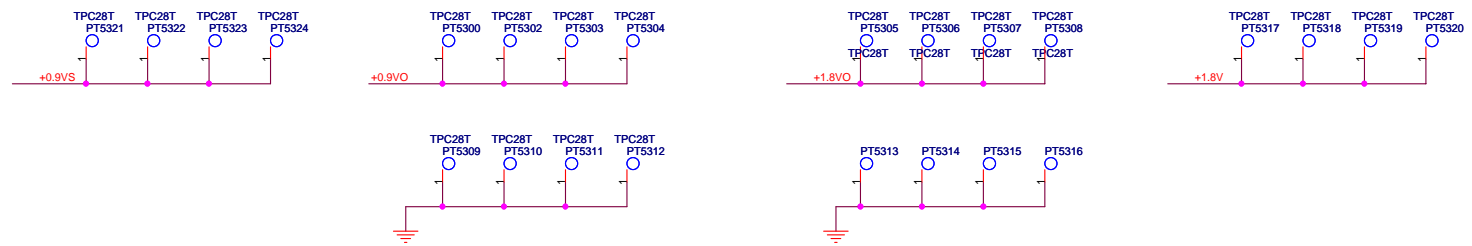
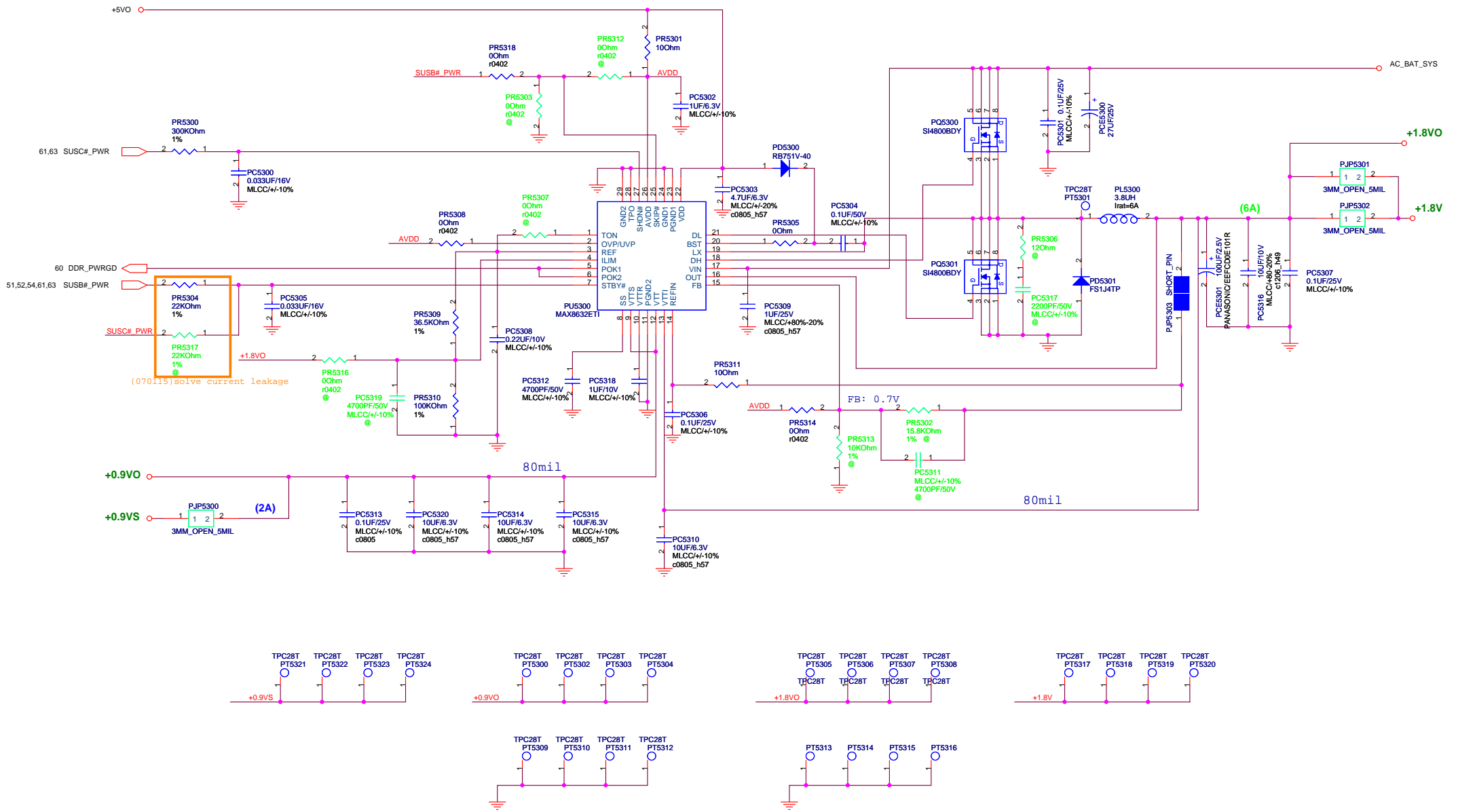
Close to Pin 18 For load line issue

C5028 & C5029 for transient response

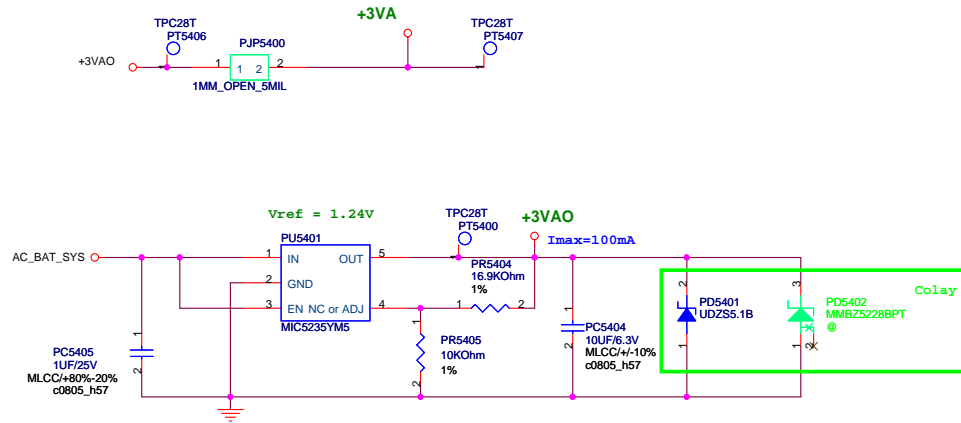
Close to Phase 1 Inductor

ASUS ALPHA		Title : POWER_VCORE	
ASUSALPHAtek COMPUTER INC.		Engineer: Amos Yu	
Size	Project Name	Rev	
Custom	TERESA	1.1	
Date: Monday, February 05, 2007	Sheet	50	of 57

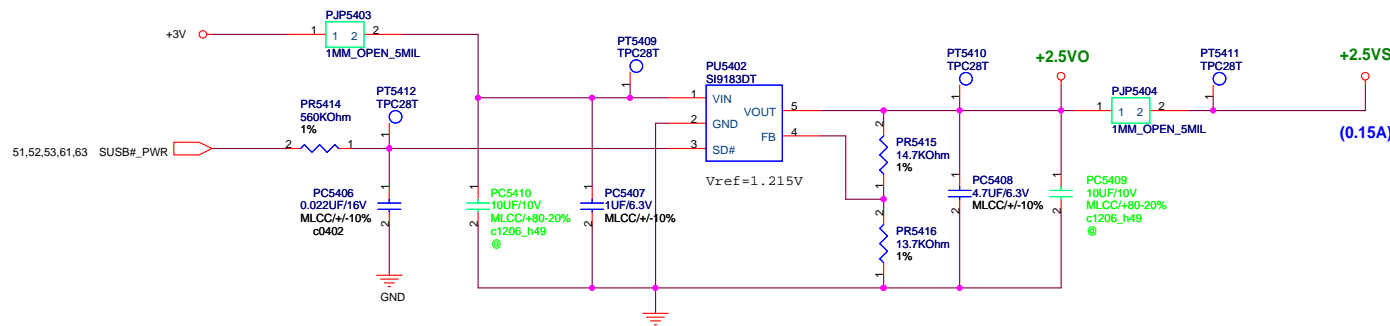




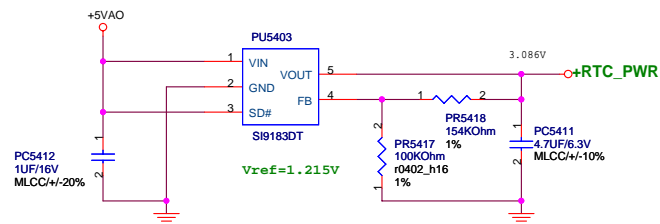
+3VAO



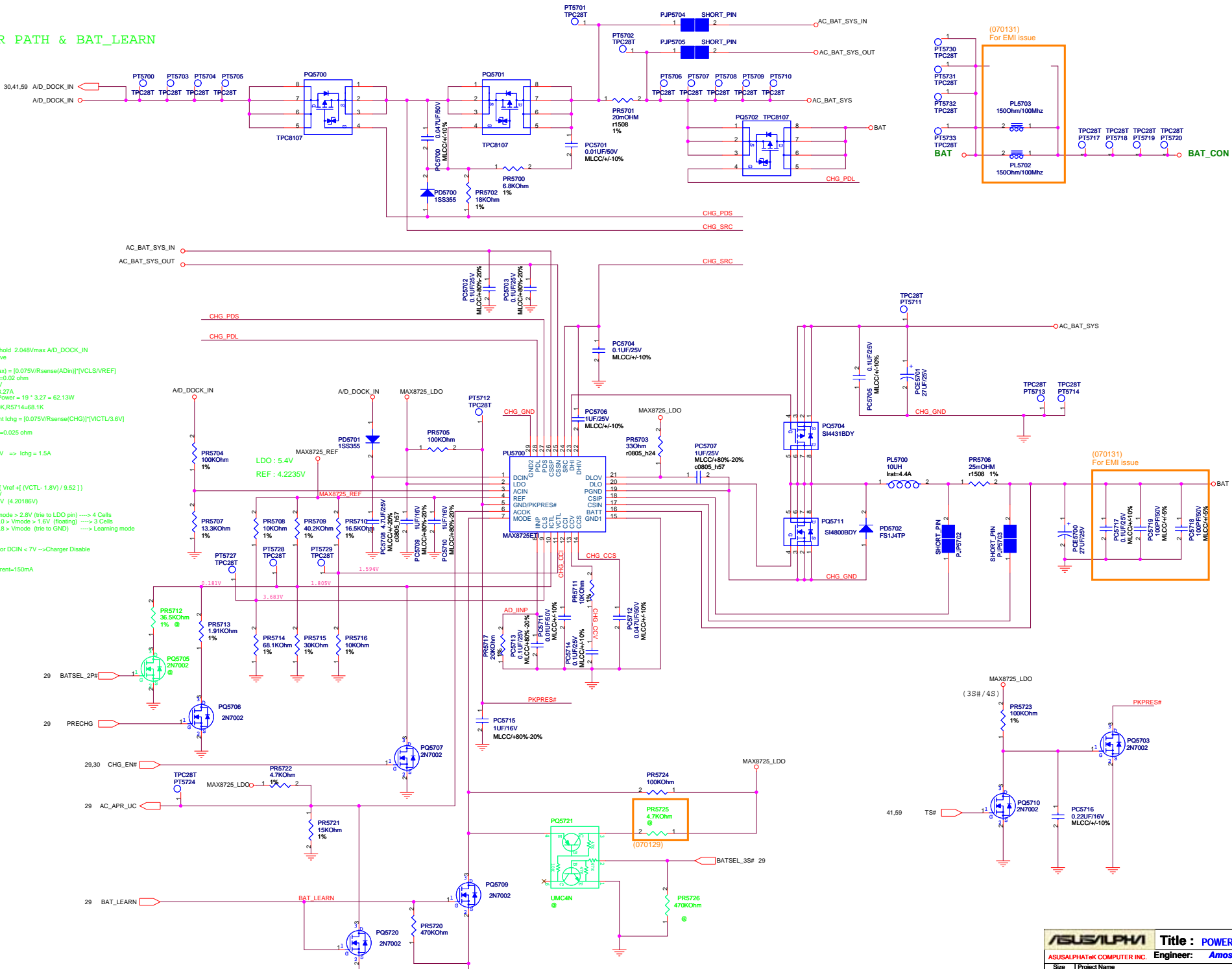
+2.5VS



+RTC_PWR

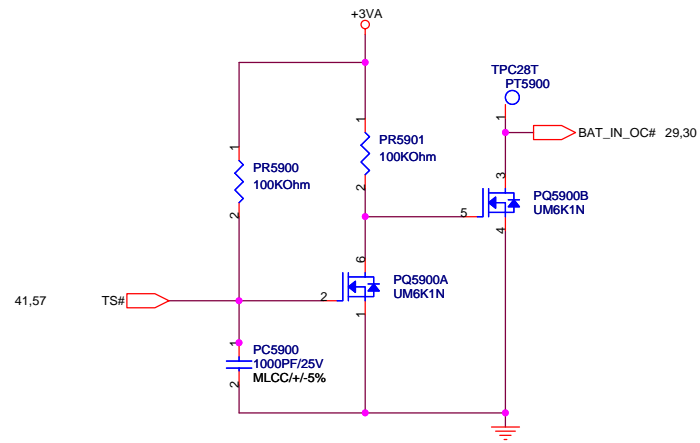


POWER PATH & BAT_LEARN

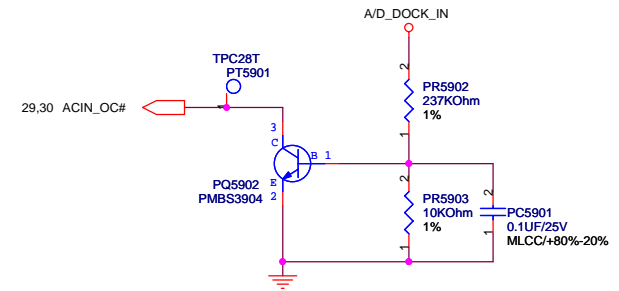


- AC_IN Threshold $2.048 \times V_{max} AID_DOCK_IN > 17.44V$ active
- Adapter $I_{in(max)} = [0.075V/R_{sense}(A_{in})] \times [V_{CL}S \times V_{REF}]$
 $R_{sense}(A_{in}) = 0.02 \text{ ohm}$
 $V_{CL}S = 3.683V$
 $\Rightarrow I_{in(max)} = 3.27A$
 $\Rightarrow \text{Constant Power} = 19 \times 3.27 = 62.13W$
 $\Rightarrow R5708 = 10K, R5714 = 68.1K$
- Charge Current $I_{chg} = [0.075V/R_{sense}(CHG)] \times [VICTL/3.6V]$
 $R_{sense}(CHG) = 0.025 \text{ ohm}$
 $VICTL = 1.805V \Rightarrow I_{chg} = 1.5A$
- $V_{batt} = Cell * (V_{ref} + [(VICTL - 1.8V) / 9.52])$
 $VICTL = 1.804V$
 $\Rightarrow V_{batt} = 4.2V (4.20186V)$
- Mode pin : $V_{mode} > 2.8V$ (tie to LDO pin) \rightarrow 4 Cells
 $2.0 > V_{mode} > 1.6V$ (floating) \rightarrow 3 Cells
 $0.8 > V_{mode}$ (tie to GND) \rightarrow Learning mode
- $VICTL = 0.8V$ or $DCIN < 7V \rightarrow$ Charger Disable
- Precarge current = 150mA

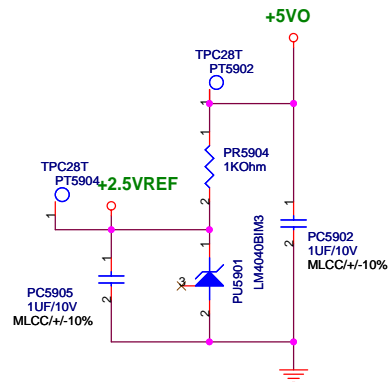
BATTERY IN DETECT



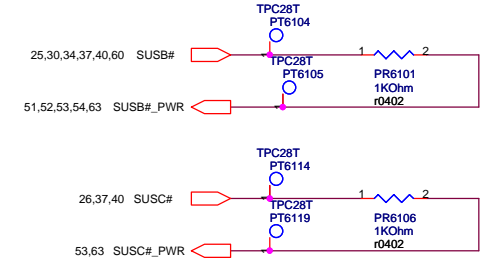
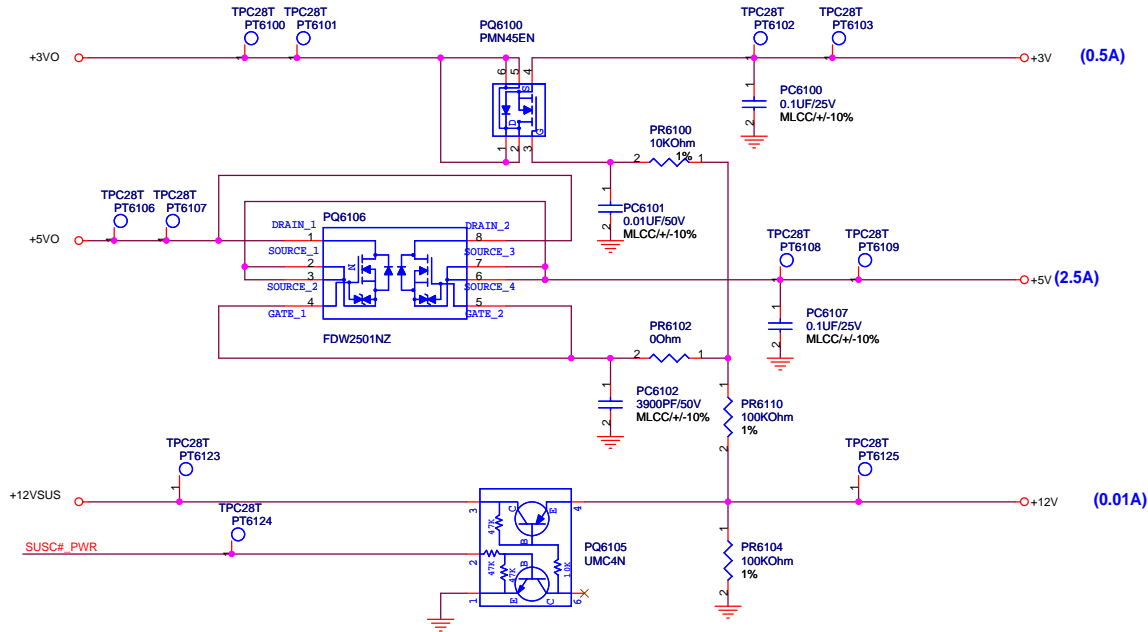
ADAPTER IN DETECT



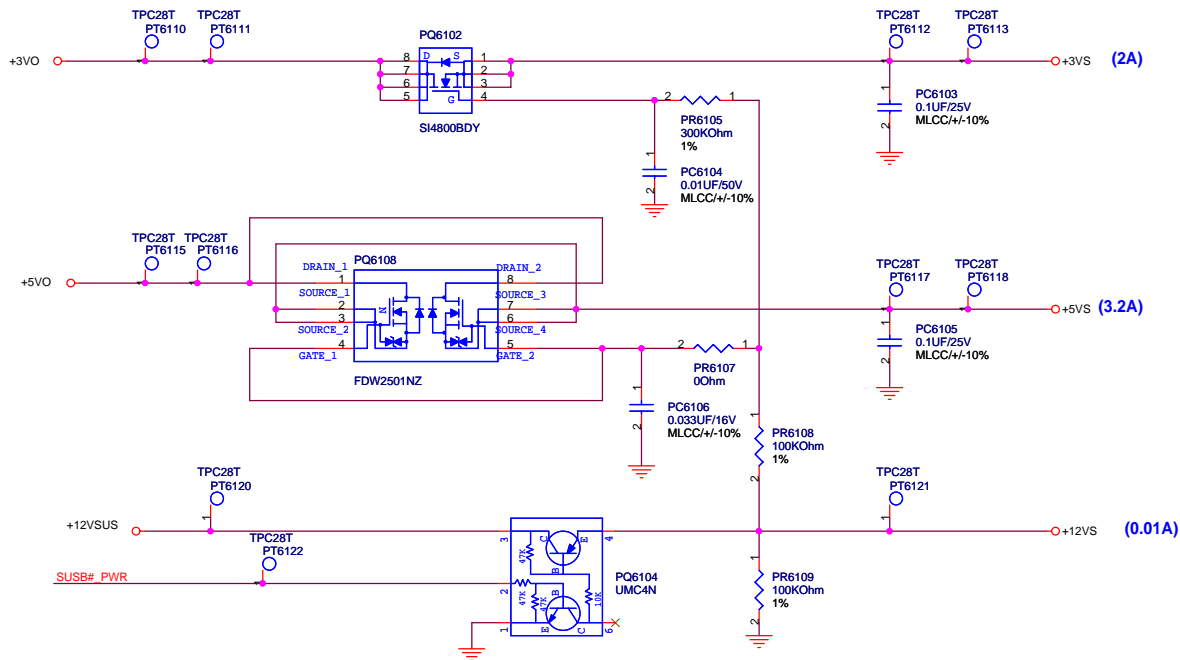
+2.5VREF

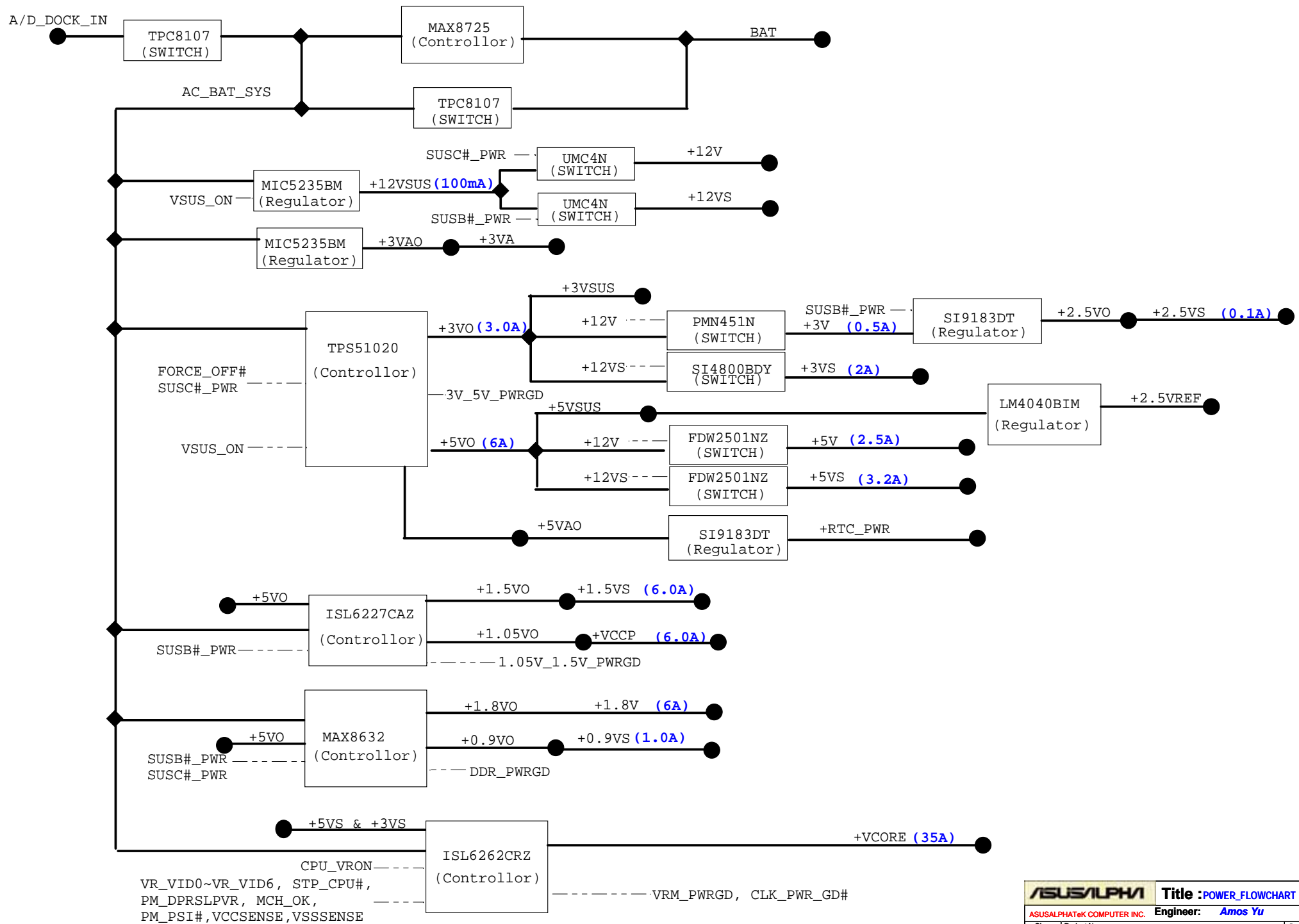


SUSC#_PWR POWER



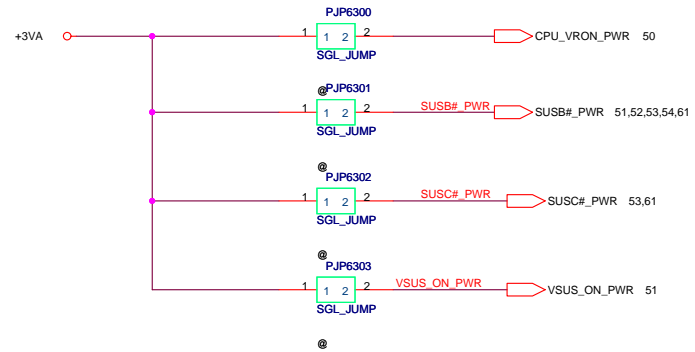
SUSB#_PWR POWER



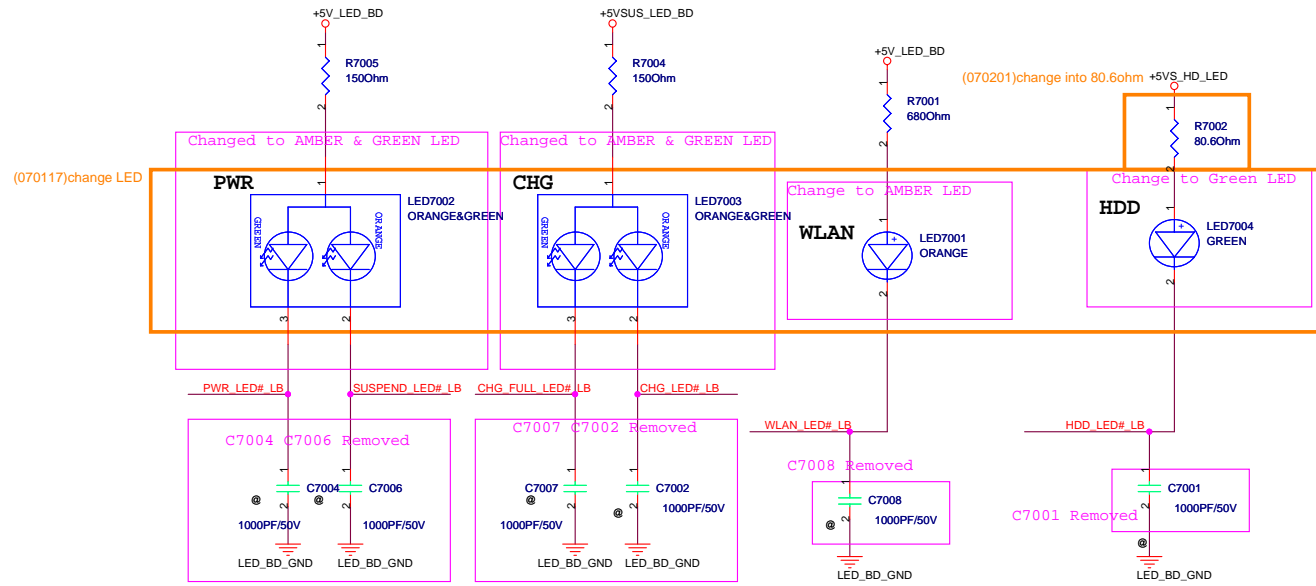




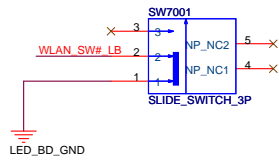
FOR POWER TEST



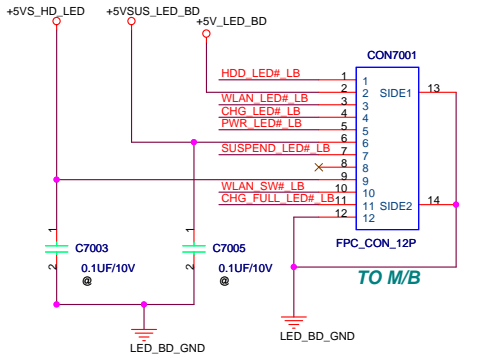
LEFT & RIGHT Button remove to TP BOARD



New added SW for Teresa

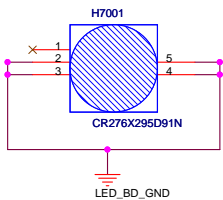


070115 Change pin define

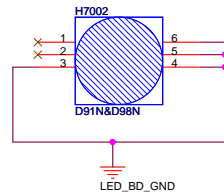


CON to T/P remove to TP BOARD

IR receive module removed



DETAIL: Q



DETAIL: S

